FR-10120

A Final Report for:

RADIATION-HARD HIGH-EFFICIENCY InP SPACE SOLAR CELL DEVELOPMENT

Submitted Under:
Contract N00014-89-C-2148

Submitted to:
NAVAL RESEARCH LABORATORY
4555 Overlook Avenue SW
Washington, DC 20375-5000

spire

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4555 Overlook Avenue SW

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Submitted by:

SPIRE CORPORATION

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TECHNICAL ABSTRACT

The efficiency of InP cells was improved to 19.1% AM0, using a cell fabrication process amenable to scale-up to production levels, and increasing the cell area to 4 cm^2. An n+/p/p+ shallow-homojunction structure, fabricated by metalorganic chemical vapor deposition was used for this work. The emitter thickness was in the neighborhood of 30 nm, and a graded doping profile (front-surface-field) was used. Two hundred cells and two complete 20-cell panels were fabricated for space flight tests. Thermal cycling and radiation tests were carried out on these cells.

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SECTION 1

INTRODUCTION AND SUMMARY

This is the final report for Phase I of research contract number #N0014-89-C-2148 between the Naval Research Laboratory, Washington, DC, and Spire Corporation, Bedford, Massachusetts, covering the period from May 15, 1989 to May 31, 1991. The principal investigator at Spire, and author of this report, was Christopher J. Keavney. The Contracting Officer's Technical Representative at NRL was Richard L. Statler. Subcontract work at the Solar Energy Research Institute was directed by Timothy Gessert. This report contains a description of all technical accomplishments made during this period, a detailed description of the state-of-the- art InP solar cell and associated processing methodology which were developed, summaries of results of all electrical and mechanical tests performed, and a discussion of areas for future development.

1.1 BACKGROUND

In 1984 it was discovered that InP solar cells show greater resistance to radiation damage than comparable GaAs cells. Potentially useful low-temperature annealing behavior was also reported, including annealing by exposure to light and current injection. This has led to considerable interest in the material for powering satellites in high-radiation orbits.

After this discovery, the development of high-efficiency InP-based solar cell structures proceeded quickly. Workers at Spire and elsewhere reported high-efficiency cells by a array of different processes. (See Section 2.1.2 below.) The highest efficiency previous to the work reported here was 18.8%, achieved at Spire with an 0.25 cm^{-2} cell, using a hybrid ion implanted/ epitaxial structure.

1.2 CONTRACT GOALS

The objective of this contract was to develop the technology to fabricate large area, high-efficiency, radiation resistant space-quality solar cells, and to verify by measurements and experiments that the goals of high efficiency, radiation hardness, and annealing of radiation damage are being met. The issues of space quality of the InP solar cells were to be verified by appropriate standard tests by Spire to ensure electrical and mechanical stability and integrity of the solar cells, with particular attention given to insure electrical contact stability. Groups of InP solar cells were to be delivered to the government for independent evaluations.

Spire was to fabricate two solar cell panels on government-furnished aluminum honeycomb-core substrates, and deliver them to the government for test and evaluation for a satellite experiment.

1.3 SUMMARY OF RESULTS AND CONCLUSIONS

The contract goals were all accomplished successfully. Solar cell efficiencies of up to 19.1% on 4 cm^2 cells were verified by independent measurements at NASA Lewis Research Center. Over 200 4 cm^2 InP cells were delivered to the government during the course of the contract, including two complete panels of 20 cells each.

The cell structure was investigated in detail, in order to achieve the highest possible efficiency while preserving the radiation resistance as far as possible. The most important variable was found to be the emitter thickness. Since light is absorbed very strongly in the emitter, and the front surface has a high recombination velocity, high efficiency can best be achieved by making the emitter very thin (about 30 nm), and using a graded doping profile (front surface field) to move the carriers toward the junction. The effects of emitter doping, base thickness, and base doping were investigated as well. Cells with low (3×10^{15} cm^{-3}) base doping showed interesting behavior during radiation tests; under the influence of compensation by radiation-induced defects, they developed a very wide (1.5 micron) space-charge region.

A front surface cap layer of $In_{0.53}Ga_{0.47}As$ was added to the structure as well; it facilitates making contact to the front and results in more reproducible diode characteristics. A chemical etching process is used to remove the cap after cell fabrication.

During the course of the contract, extensive work was done on the development of a cell fabrication process which would be amenable to scaling up to production levels. The first step was to eliminate the ion implantation and anodization steps which had been used before for the highest-efficiency results. This was accomplished by developing sufficient control over the MOCVD growth process that a thin (30 nm) emitter layer could be grown reproducibly and uniformly with a graded doping profile. By this method, the entire cell structure could be grown in one process.

More reliable front and back contact processes were developed as well. For the front contact, the effect of evaporation conditions (chiefly the wafer temperature) on the stress in the metal film was investigated in order to prevent peeling of the 5 micron thick silver contacts. Contact adhesion sufficient to pass the tests described in the contract was achieved, although subsequent experience indicates that yield could be improved by a further increase in adhesion strength. For the back contact, more reproducible evaporation and annealing procedures were developed; instead of a graphite strip heater, the contacts were annealed in a tube furnace, allowing several wafers to be processed at a time.

Considerable attention was also paid to panel fabrication processes. The antireflection coating was redesigned for use with a coverglass. Thermosonic bonding was identified as the most reliable process for attaching contact ribbons to the front of the cells, and conditions which resulted in the most consistent pull strength were found. Bonding of coverglasses, soldering of the cells into strings, and assembly of panels were carried out.

Yield of the cell fabrication process followed a predictable pattern: low yield would often characterize a new process step for the first several tries. Then, as further experience was gained with the process, yield would improve and become reliable. At the end of this project, high yields (75% overall) were achieved in all of the early steps of the process up to the beginning of panel fabrication. For the steps leading up to panel fabrication, yields were somewhat lower and some further work is needed.

Thermal cycling tests were carried out on two individual covered cells and on the two panels. No damage was observed. Radiation and annealing tests were done on 35 individual cells up to 10^{16} cm^{-2} electrons at 1 MeV. The highest post-irradiation efficiencies measured were 15.6% after 10^{15} cm^{-2} and 12.0% after 10^{16} cm^{-2}. Annealing at 140°C increased the efficiency of cells with a dose of 10^{16} cm^{-2} from 12% to 14%.

SECTION 2

BACKGROUND

2.1 PRINCIPLES OF HIGH-RADIATION-RESISTANCE InP SOLAR CELLS

2.1.1 Properties of InP

Indium phosphide (InP) is a cubic semiconductor very similar to gallium arsenide. Its bandgap (1.35 eV) is slightly smaller, but larger than that of silicon. In its mechanical, crystallographic, and chemical properties it resembles GaAs very closely, with one exception: while the two elements making up GaAs are very close in atomic weight, InP is a compound of a heavy metal (indium) with a relatively light non-metal (phosphorus). As explained in Section 2.1.3, this gives the material certain advantages in radiation resistance.

InP is produced in single-crystal wafer form by the liquid-encapsulated Czochralski process, as is GaAs. The cost is somewhat higher (about $\$10/cm^2$ as of this writing), for two reasons: higher pressures are needed during the growth, and the market is much smaller.

2.1.2 InP Solar Cells - High Efficiencies

A number of investigators[1-5] have addressed the question of the maximum theoretical efficiency of a solar cell as a function of bandgap. The calculations of Wysocki and Rappaport[4] predict an efficiency of 26.5% for GaAs and 26% for InP (at 25° C, one sun AM0). On the other hand, more recent analyses,[1,2] using a more fundamental approach, show a peak efficiency of 29% at a direct bandgap near 1.3 eV, indicating a predicted efficiency for InP slightly higher than that of GaAs. Considering the number of unknown variables involved, we can only conclude that the theoretically attainable efficiencies of InP and GaAs are the same for practical purposes, and that the higher efficiencies demonstrated with GaAs cells are a result of the great investment which has been made in the technology over the years, not of any fundamental reason.

Because of the higher cost of InP, it was not considered of great interest for this application until the relatively recent discovery of its superior radiation resistance.[6,7] It was found that high-energy radiation, as encountered in orbit, causes less damage to the performance of InP cells than to silicon or GaAs cells. These results were confirmed by other workers.[8] It also appears that much of this damage can be recovered at a relatively low temperature.[9-11]

After this discovery, the development of high-efficiency InP-based solar cell structures proceeded quickly. Yamamoto[7,12] reported high-efficiency cells by a diffusion process, while Coutts and Naseem[13] achieved remarkable results with a simple sputtered indium tin oxide heterojunction. Ghandi[14] used another diffusion technique. Higher-efficiency cells have been formed by MOCVD;[15-18] these include p on n structures of 15.6% efficiency[16] and n on p structures of 17.9%.[17] A hybrid epitaxial/implanted structure was used to achieve 18.8% at Spire in 1987.[19] Production of more than one thousand cells of 2 cm^2 area has been carried out by diffusion.[20]

2.1.3 Radiation Resistance

The original publications by Yamaguchi and others at Nippon Telegraph and Telephone[6,7] in 1984 reported less damage to InP cells than to comparable GaAs cells under gamma radiation (Figure 2-1). Although only the relative efficiencies were compared, measurements were also made of the diffusion length changes, and the damage constant (change in inverse square of diffusion length with gamma ray dose) was found to be 5 to 15 x 10^{-11} for InP (depending on the doping level), compared to 5.7 x 10^{-10} for GaAs. These results have been reproduced at other laboratories, and the relative damage rates have been found to be similar for electron and proton radiation as well.[8] Weinberg and Brinker[21] did some calculations based on these and other measurements which indicated considerably higher end-of-life efficiencies for InP cells in various orbits.

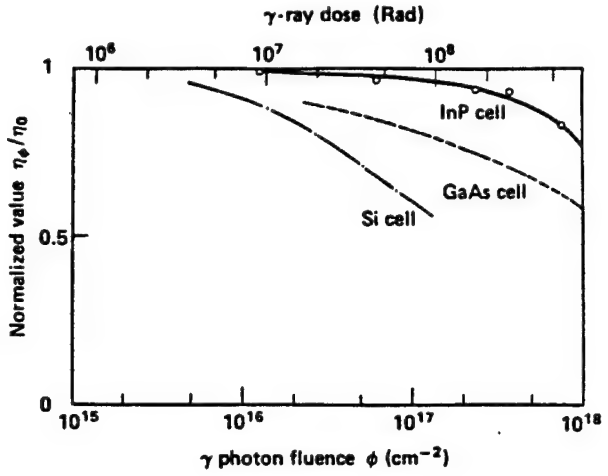


Figure 2-1 *Comparison of radiation damage in solar cells of InP, GaAs, and Si.*

Although the preliminary results[6-12] are encouraging, most of the reports have given only relative decreases in efficiency, without stating the original efficiency or other parameters of the cells that were tested. Since cells of low efficiency are generally degraded less by radiation, it remained to be seen how much degradation would be found in cells with an efficiency comparable to that of GaAs.

Two factors are expected to contribute to the high radiation resistance of the InP cell. First, due to the higher optical absorption coefficient over most of the solar spectrum, the active volume of the cell is thinner, and so a smaller diffusion length is required for good current collection; thus reduction in the diffusion length due to radiation has a smaller effect.

Figure 2-2 shows the carrier generation rate as a function of depth for InP and for GaAs under AM0 illumination. The advantage of InP can be clearly seen: since more carriers are generated in a smaller volume of the cell, higher efficiency can be realized with the same diffusion length.

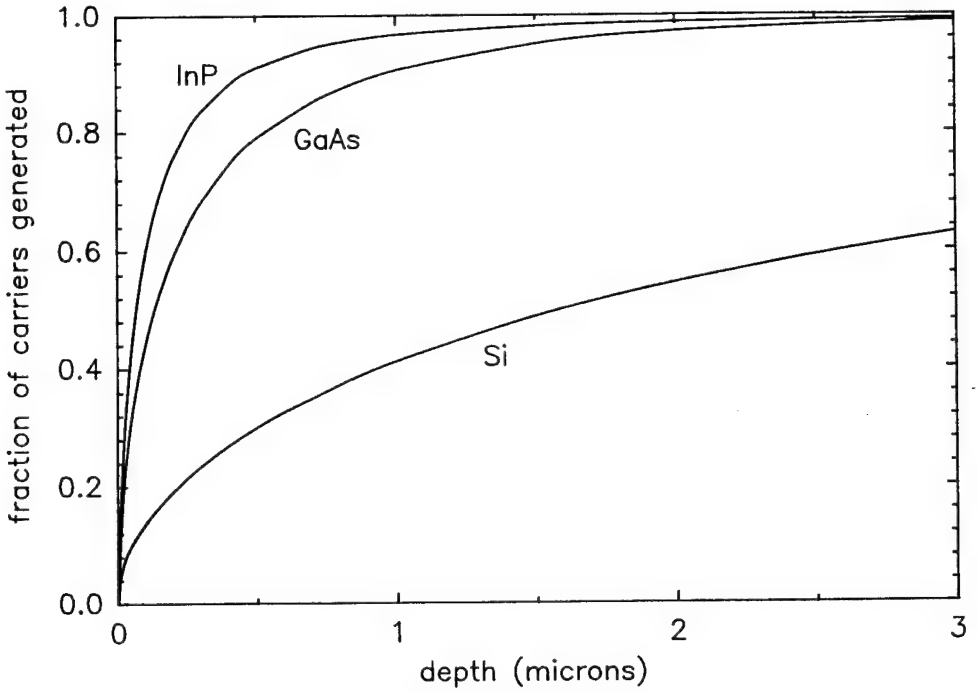


Figure 2-2 *Carrier generation rates in InP, GaAs and Si under AM0 illumination. The higher absorption coefficient of InP is one of the factors leading to increased radiation resistance.*

Aside from this, however, the measurements show that the reduction in carrier diffusion length for a given dose is also less in InP than in GaAs, and recovery takes place at a lower temperature. Yamaguchi and Ando[11] briefly discuss the atomic nature of the defects in InP, concluding that the most important trap level (designated H4) is a phosphorus Frenkel pair. The relatively low activation energy for annealing of this defect is presumably due to the relatively high mobility of phosphorus atoms in the InP crystal lattice; because of their small size, they can more rapidly move back into position after being displaced by a collision with a high-energy particle. The damage coefficients which he measured for various InP and GaAs cells are shown in Figure 2-3.

In any case, it appears that the observed high radiation resistance is inherent to InP and is not an artifact of a particular cell structure. These data indicate that, if beginning-of-life efficiency close to that of GaAs is achieved, InP has the promise of higher end-of-life efficiency than any other material.

2.2 STATUS OF InP SPACE CELL TECHNOLOGY

Up to this point, the highest efficiencies have been achieved with shallow homojunction designs (Figure 2-4). In this design, the emitter layer is made as thin as possible to allow most of the current to be absorbed in the space-charge region and the base. Although some of the carriers generated in the emitter are collected, the fraction is lower than that for the base, because of recombination either at the front surface or in the heavily-doped region itself. Therefore, the short-circuit current of the cell is strongly dependent on the emitter thickness. Figure 2-5 demonstrates this strong dependence by comparing the spectral responses of epitaxial cells with different emitter thicknesses.

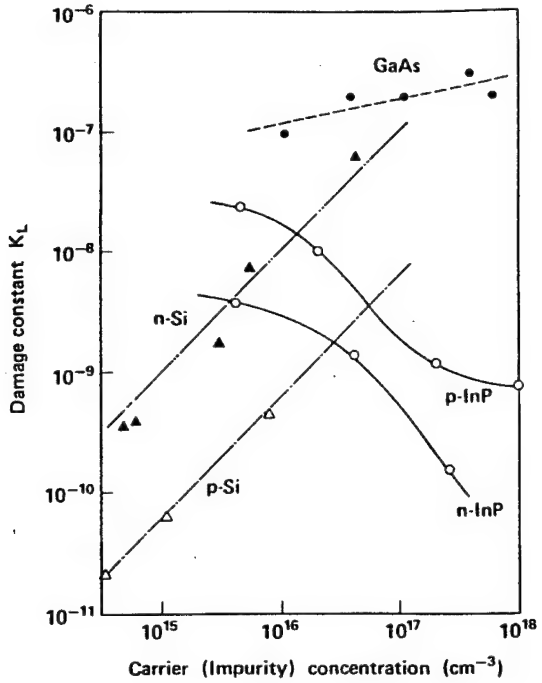


Figure 2-3 *Damage coefficients in InP and GaAs solar cells. (From Reference 11).*

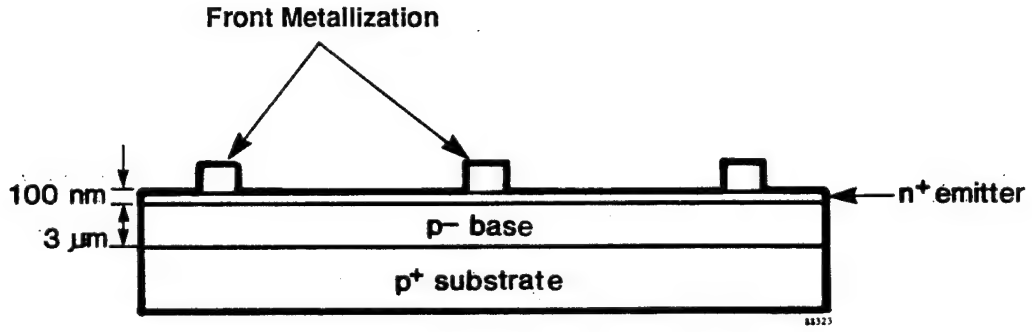


Figure 2-4 *Shallow homojunction cell design. The emitter is made as thin as possible to allow most of the current to be absorbed in the space-charge region and the base.*

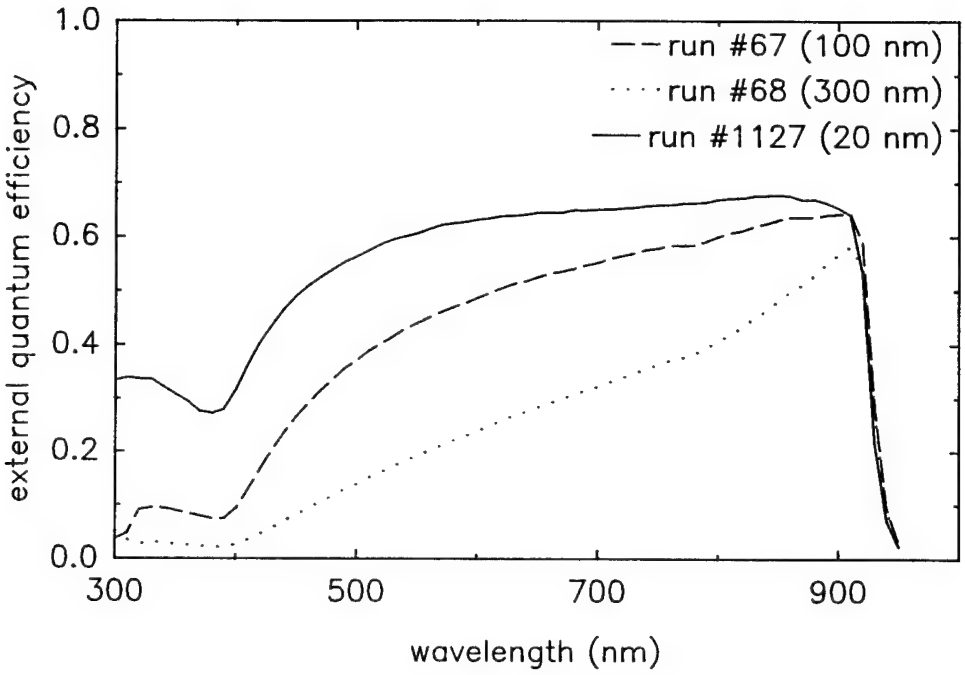


Figure 2-5 *Effect of emitter thickness for epitaxial cells. Emitters thicker than a few hundred angstroms result in greatly reduced blue response.*

The other approach to high efficiency, which has been successful with GaAs cells, is to use wide-bandgap window layers to reduce the recombination at the surfaces (Figure 2-6), according to the same principle which is used for heterostructure lasers. The possibility of applying this to InP will be discussed in Section 6.2.

Although much research had been devoted to the junction formation technologies such as diffusion and epitaxy, until the present work the other areas of cell fabrication (metallization, space qualification, and assembly into modules) had received relatively little attention.

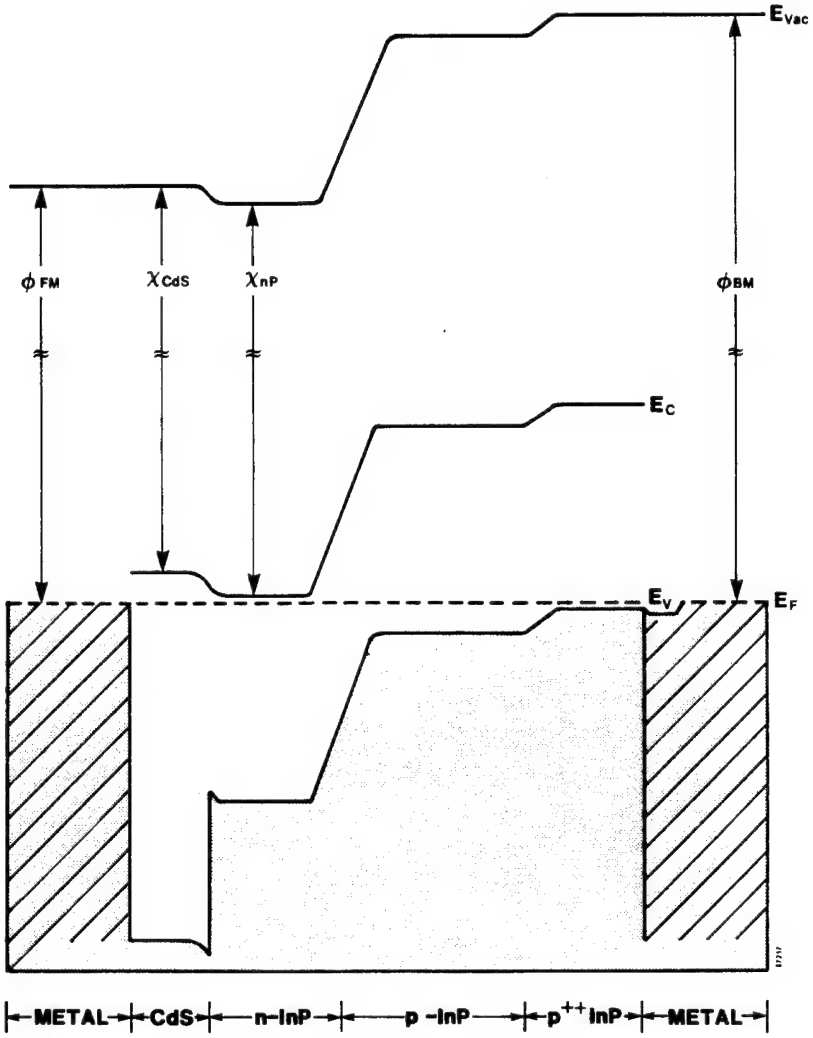


Figure 2-6 *Band diagram for the InP solar cell with CdS window layer. The large discontinuity in the valence band at the front surface confines the photogenerated holes.*

SECTION 3

PROCESS DEVELOPMENT

3.1 BRIEF OUTLINE OF PROCESS

The first step in making the InP solar cell is the formation of the p-n junction. In this work, the method used was to begin with a heavily-doped p-type InP substrate and grow all of the active layers of the cell by metalorganic chemical vapor deposition. In the course of previous work, this approach was compared to various alternatives (ion implantation, sputtering of indium tin oxide, use of the substrate as one active layer), and found to give the highest efficiency.

Next, ohmic contacts must be made to the n-type and p-type regions of the cell. The research here concentrated on photolithography and evaporated metal, which have been the standard methods for manufacture of space solar cells of all types.

Antireflection coating was also carried out by evaporation. Interconnecting ribbons were bonded to the cells by the thermosonic technique, and coverglasses were applied with an adhesive.

The following section discusses the experiments done during this project with the process and the changes made as a result. The next section reviews the current process in detail.

3.2 PROCESS DEVELOPMENT EXPERIMENTS

3.2.1 Emitter Growth Rate - Thickness Control

Previous work[17,22] had shown that one of the most important variables in determining the cell efficiencies was the thickness of the emitter. Thicknesses on the order of 20 nm are required for optimum efficiency. Producing layers by MOCVD of that thickness with good control and reliability, although possible, requires some development. Previous to this work, cells had been made by growing the emitter 100 nm thick and then reducing the thickness by anodic oxidation.[17] While successful in some cases, this technique is not easily amenable to production, is not highly reproducible, and is not compatible with the graded-doping profiles desired (see Section 4.2.2.). Accordingly, we undertook to develop an all-epitaxial process for producing the same structure.

With this end in view, a series of modified emitter structures was grown. First, the growth rate for the emitter portion of the cell was reduced from 1.1 nm/sec to approximately 0.15, to allow better control of the doping profile. Then, a series of runs at approximately the same doping concentration but different emitter growth times was made, to observe the relation between growth time, emitter thickness, and sheet conductivity. After this was done, the three emitter structures described in Figure 3-1 were grown, along with a control wafer. These wafers were processed into cells and tested; the results, which are given in Table 3-1 below, show that the performance of the one-step MOCVD-grown emitter is essentially equal, with greater uniformity, to that of the anodized emitter, and the two-step emitter structure yields a significantly higher short-circuit current and blue response than the control.

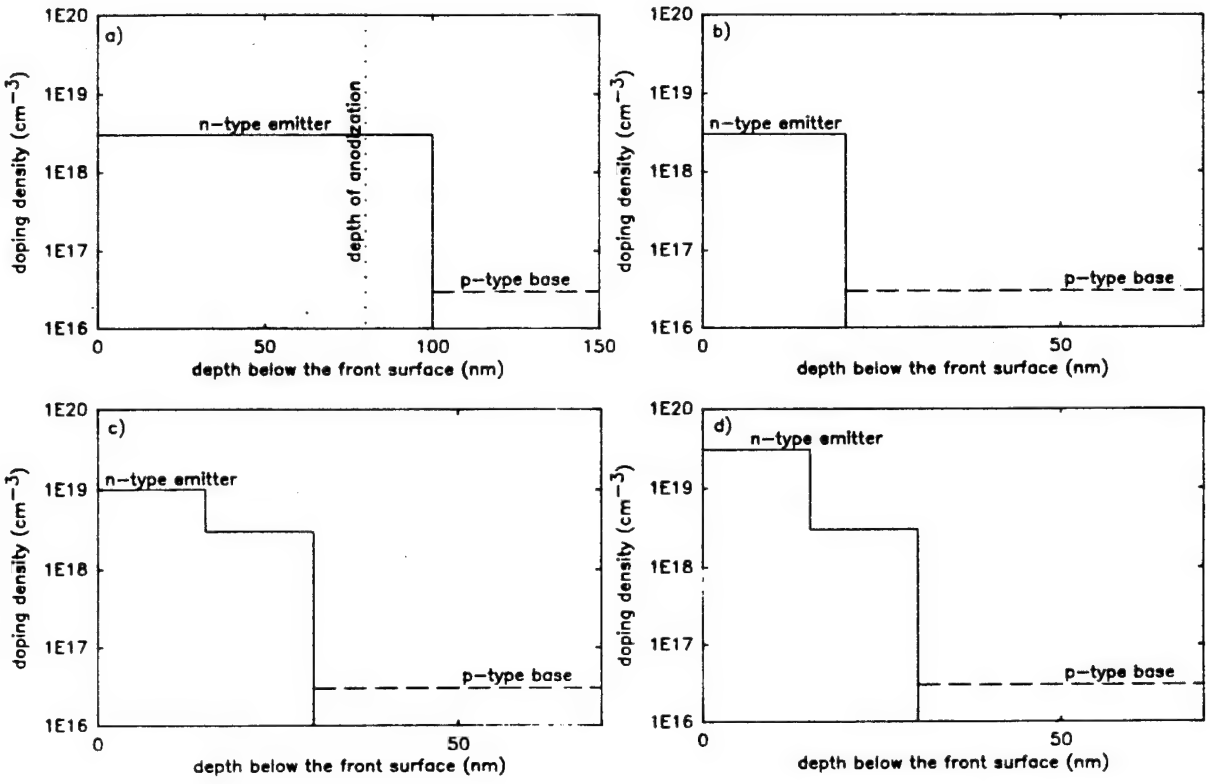


Figure 3-1 *Emitter structures grown during this project. a) Standard emitter structure. The emitter is grown 100 nm thick and then etched to 20 nm. b) One-step thin emitter. A slower growth rate is used, and the emitter is grown to 20 nm thickness, eliminating the need for etching. c and d. Two-step thin emitters. The higher doping near the surface creates a field which improves the collection of carriers.*

Table 3-1 *Short-Circuit Currents of Lot 5271 (Study of thin MOCVD-grown emitters).*

	Short Circuit Current (mA/cm^2)	*Internal q.e. @ 400 nm*
control group (anodized emitter)	21.65 $\pm$ 0.83	
run # 899 (one step emitter)	21.14 $\pm$ 0.35	0.34
run # 904 (two-step emitter)	22.89	0.48
run # 905 (two-step emitter)	23.52 $\pm$ 0.38	0.56

These structures were characterized by differential Hall effect measurements; the results for one run are shown in Table 3-2. Although there is considerable scatter in the data due to the small thicknesses involved, the results indicate that the actual doping profile in the emitter is acceptably close to the desired one.

Table 3-2 *Differential Hall Measurement of Run #905.*

Step #	Depth (nm)	Dopant Concentration (cm^{-3})
1	0-6	1.3×10^{19}
2	6-11	2.7×10^{19}
3	11-17	7.0×10^{18}
4	17-23	4.8×10^{18}

Measurements of the sheet resistance were made on some wafers, to determine the variation in the emitter with position on the wafer; results are shown in Figure 3-2.

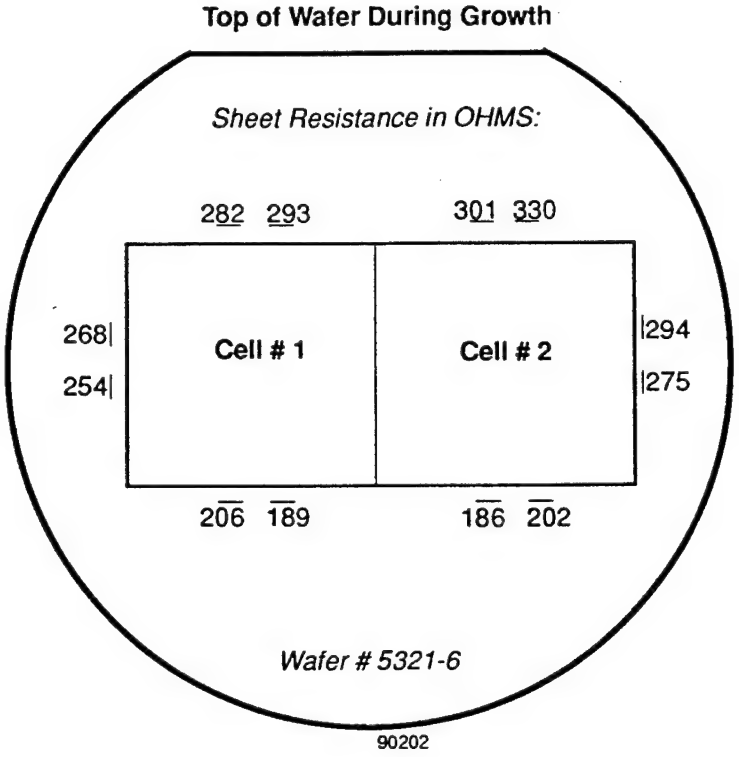


Figure 3-2 *Measurements of the sheet resistance on an InP cell wafer. Considerable variation is seen, but the measured values are within the design limits.*

Figure 3-3 shows the variation from run to run of the quantum efficiency in the blue end of the spectrum, which is primarily determined by the emitter thickness. The mean of these measurements is 0.593 and the standard deviation 0.025. Due to the very high sensitivity of the blue response to this parameter, the variation seen here indicates a very small variation in the emitter thickness.

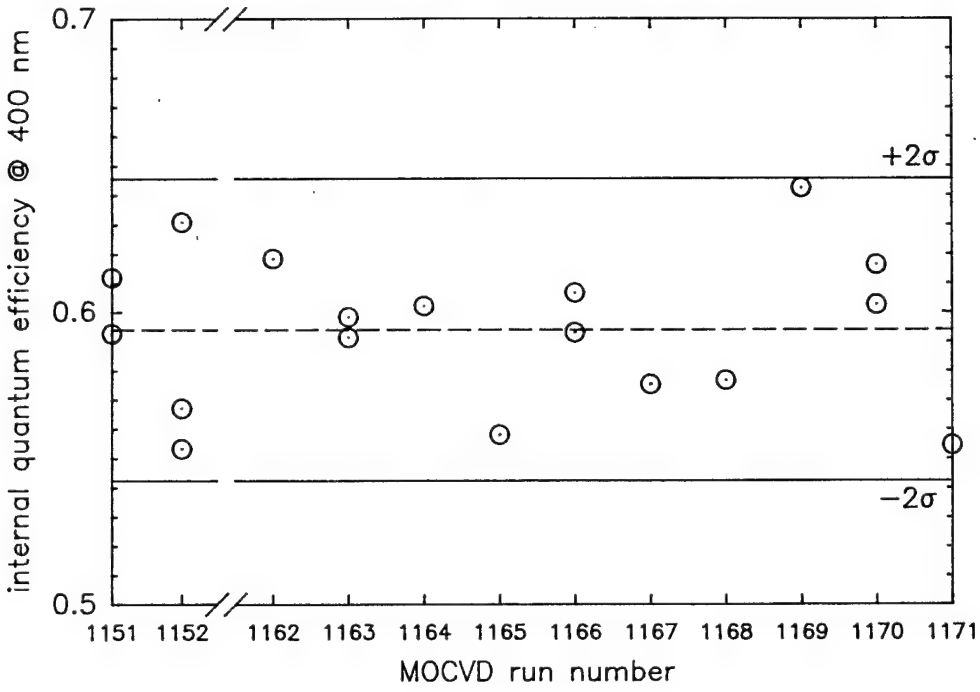


Figure 3-3 *Variation of blue response from run to run. Over 12 runs, the quantum efficiency at 400 nm varied from 0.55 to 0.64; considering the high sensitivity of the response to the emitter thickness, this indicates a very small thickness variation.*

3.2.2 Growth Temperature

The temperature of MOCVD growth has proved to be one of the important parameters in the growth of GaAs solar cells. Accordingly, we investigated its effect in the growth of InP solar cells.

The baseline growth temperature for the cell growth was 600°C; in the first experiment we grew some cells at 640°C and compared them to controls grown at 600°C. The results, shown in Table 3-3, indicate that the cells grown at a higher temperature are markedly lower in efficiency than the controls.

However, the higher temperature also resulted in a lower base doping concentration, due to the changing characteristics of the reactions responsible for the incorporation of zinc into the InP. Since the change of doping level may itself have an effect on the efficiency, we did another growth run to separate the effects. In this run, the temperature was 640°C, but the Zn flow was increased to give the same base doping concentration as the controls. Table 3-3 shows that the efficiency is still low.

Table 3-3 *Effect of Growth Temperature. (Lots 5381, 5384)*

MOCVD growth run #	Growth Temp. (°C)	DMZn flow rate (sccm)	Before AR Coating				AMO Eff. (%)	After AR Eff.
			Base doping (10^{16} cm^{-3})	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)		
1111	600	10^{-5}	5.9 ± 1.0	878 1	23.65 0.04	0.838 0.001	12.7 0.1	19.1
1113	640	10^{-5}	0.87 ± 1.3	802 62	24.63 0.22	0.785 0.038	11.3 1.5	16.6 2.0
1124	600	10^{-5}	2.9 ± 0.4	872 1	24.27 0.10	0.848 0.005	13.1 0.1	17.7 0.1
1125	640	$6x10^{-5}$	4.3 ± 1.6	761 16	24.49 0.09	0.763 0.006	10.4 0.3	14.0 0.4

We concluded, therefore, that a higher growth temperature is detrimental to the process, possibly because of the loss of phosphorus from the surface. All subsequent growth runs were done at 600°C.

3.2.3 Wafer Size, Shape and Supplier

In order to determine the most efficient way of using substrates, we investigated the effect of wafer size, by comparing cells made on 56 mm wafers to those made on standard 50 mm wafers. Since two 20 mm square cells are made on each wafer, the distance from the corner of the cell to the edge of the wafer was 2.6 mm for the 50 mm wafer, and 5.6 mm for the larger size. Since the area near the edge of the wafer tends to suffer from a high defect density (for a number of reasons), we used the larger wafers for most of the work under this contract, but compared the results to those obtained with the standard size. It was found that the difference in efficiency with wafer size was barely significant (see Table 3-4).

We also made some cells on 45 mm square substrates. (We obtained these substrates by cutting 75 mm round wafers.) Four cells could be made on each substrate in that case, but these cells had significantly lower efficiency than the controls made on 56 mm diameter wafers. The reason for this is not known.

Finally, we also compared the performance obtained with four substrate suppliers. Wafers from one of the suppliers produced cells with relatively low efficiency; these wafers also had poor surface quality after growth, presumably due to subsurface polishing damage. At the manufacturer's recommendation, some of these wafers were etched before growth; no significant improvement was seen. No significant difference was found among the other three suppliers.

Table 3-4 *Effect of Wafer Size and Supplier.*

MOCVD growth run #	Supplier	Size (mm)	Before AR Coating				After AR Eff. (%)
			V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	AMO Eff. (%)	
1059-63	S	56	873	23.58	83.1	12.5	18.5
(7 cells)			± 3	0.68	0.8	0.2	0.1
	N	50 sq.	826	22.63	80.4	11.0	15.0
(9 cells)			± 6	0.68	1.0	0.4	0.4
1108-09	S	56	875	23.72	84.4	12.8	18.4
(4 cells)			± 1	0.44	0.2	0.3	0.8
	S	50	878	23.86	83.1	12.7	18.9
(4 cells)			± 1	0.16	1.4	0.1	0.1
	N	50	872	23.80	84.3	12.7	19.0
(4 cells)			± 1	0.08	0.3	0.1	0.1
	C	51	857	23.49	81.4	11.9	17.9
(4 cells)	(not etched)		± 2	0.05	1.5	0.2	0.4
1138	S	56	871	23.79	85.2	12.9	17.7
(4 cells)			± 1	0.22	1.0	0.2	0.1
	C	51	842	23.77	81.1	11.8	n/a
(5 cells)	(etched)		± 7	0.25	0.6	0.2	
1167-70	S	56	877	24.77	83.7	13.3	18.7
(16 cells)			± 3	0.20	0.08	0.1	0.2
	N	50	878	24.77	83.7	13.3	18.7
(12 cells)			± 5	0.21	1.4	0.2	0.3

3.2.4 InGaAs Front Surface Cap

The use of an InGaAs cap layer was crucial in the reproducible fabrication of high-efficiency cells. Cap layers were used on all of the deliverable cells, and on all of the cells for which results are reported here, except where otherwise indicated.

The first cells made with cap layers showed greatly improved performance. Because these were made with thick emitters, their efficiencies were still relatively low, but the high voltages and fill factors showed that they do not suffer from the unexplained recombination which had been seen in most of the previous cells. Table 3-5 shows the measurement results from one of the first baseline lots (made without the cap), the results of the cap layer experiment, and the first lot of deliverable cells made with the cap layer.

Table 3-5 *Results of First Cap Layer Cells.*

Lot & Wafer	Emitter Thickness	Before AR Coating				After AR Eff. (%)
		V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	AMO Eff. (%)	
5281 (10 cells)	anodized (200Å) (no cap)	788 ± 27	21.72 1.62	74.2 2.5	9.3 1.0	n/a
5295-3 (2 cells)	1000Å (no cap) (controls)	814 ± 1	17.86 0.12	80.1 1.5	8.5 0.2	12.7 0.6
5295-4-1 (2 cells)	anodized (200Å) (no cap)	666 ± 1	22.41 0.18	75.3 1.3	8.2 0.1	11.9
5295-2 (2 cells)	1000Å with cap	862 ± 1	18.30 0.02	82.4 0.3	9.5 0.1	13.1 0.1
5327 (4 cells)	200Å with cap (deliverables)	871 ± 2	23.49 0.23	81.6 2.1	12.2 0.4	16.9 0.8

The addition of the InGaAs cap layer also made it possible to eliminate a step in the process. Previously, the front of the wafers had been coated with a layer of SiO_2 to protect them during the back contact evaporation and sinter. At first, this procedure was continued, and the oxide layer was deposited over the cap and subsequently removed. Although some good cells were made in this way, the first lots of deliverable cells showed low open-circuit voltage and fill factor, similar to the previous cells made without caps. Finally, when this step was removed, the cell performance improved dramatically.

The explanation which seems most likely for the previous low efficiencies is that the oxide deposition, which was done at 350°C and included rapid heat-up and cool-down steps, introduced cracks into the wafers through thermal stress. This is suggested by the great variation which was seen in those cell results; some wafers are barely affected while others are badly damaged. It also could explain why the same process was successful in earlier work, producing an 18.8% cell in 1987: the earlier work was all with small cells, and full wafers were rarely processed. However, there are other explanations which are consistent with the observations, so this hypothesis can not be considered proven.

3.2.5 Back Contact Anneal Process

Metal composition - The contacts are formed on the back of the wafers by the evaporation of zinc and gold, followed by an alloying step. It was not found to be necessary to make fundamental changes in this process, which was developed in the previous work before this contract; but minor adjustments were required.

In the preliminary work before this project, the zinc and gold were evaporated sequentially; a 3:1 ratio in weight was used to give roughly equal thicknesses (about 500Å of each metal). In this work it was found that, at least for the heavily-doped surfaces used here, a lower concentration of zinc (5% by weight) works as well, and the evaporation of the metals together, as an alloy, is equally successful. This provides a considerable advantage from the point of view of production, because it simplifies the process.

Alloying furnace atmosphere - One problem arose in this work which had not been observed previously: the back contact metal films were found to outgas during the alloying step. This had not been noticed earlier, probably because most of the previous work was with small pieces and the alloying was done in a strip heater at reduced pressure.

When the first full wafers were alloyed in nitrogen at atmospheric pressure, a bluish-brown film was found to cover the metal surface afterward. This material was later identified (by Auger spectroscopy) as a zinc-phosphorus compound. When wafers were alloyed in a vacuum furnace (either in a vacuum or at a low pressure of nitrogen), no such film was observed, but in some cases a deposit appeared on the colder end of the furnace tube, indicating that the material is volatile.

Experiments were done to find the effect of the metal composition on this outgassing. It was found in one case that reducing the zinc concentration to 5 to 10% (by weight) prevented the formation of the film, but a second trial showed otherwise.

Alloying in the vacuum furnace was adopted as the standard method for contact formation as a result of these data. Although not as simple as alloying in a tube furnace at atmospheric pressure, it is practical for production, since a tube can hold a considerable number of wafers. However, we found that it requires careful attention to the control and uniformity of the temperature.

Alloying temperature - In order to determine the acceptable range of temperatures for the alloying process, and to gather data which may be needed in the future for further process changes, we characterized the effect of alloying temperature thoroughly. First, the furnace was carefully profiled using thermocouples mounted on wafers, so that the correspondence between the measured temperature outside of the tube and the actual temperature of the wafer would be known. (See Figure 3-4). Then, test pieces of InP with Au-Zn metallization were annealed at various temperatures in the furnace. The electrical characteristics of the alloyed contacts were measured, and their appearance was recorded. These data are summarized in Table 3-6.

It was found that the Au-Zn/InP surface undergoes three distinct color changes with increasing temperature. First, a light reddish color replaces the gold; according to Fatemi,[23] this indicates the formation of Au_3In. Second, the film becomes colorless again, with the formation of $AuIn_2$. Finally, when the eutectic point is reached and the film becomes liquid, it appears more reflective and patterns of crystallization are visible after cooling.

Although previous work with lightly-doped InP substrates (about 2×10^{16} cm^{-3}) indicated that a higher temperature may be necessary for the formation of an ohmic contact, for the heavily- doped material used here (4×10^{18} cm^{-3}) any temperature above 400°C (corresponding to the formation of the reddish color) was found to give a satisfactory electrical contact.

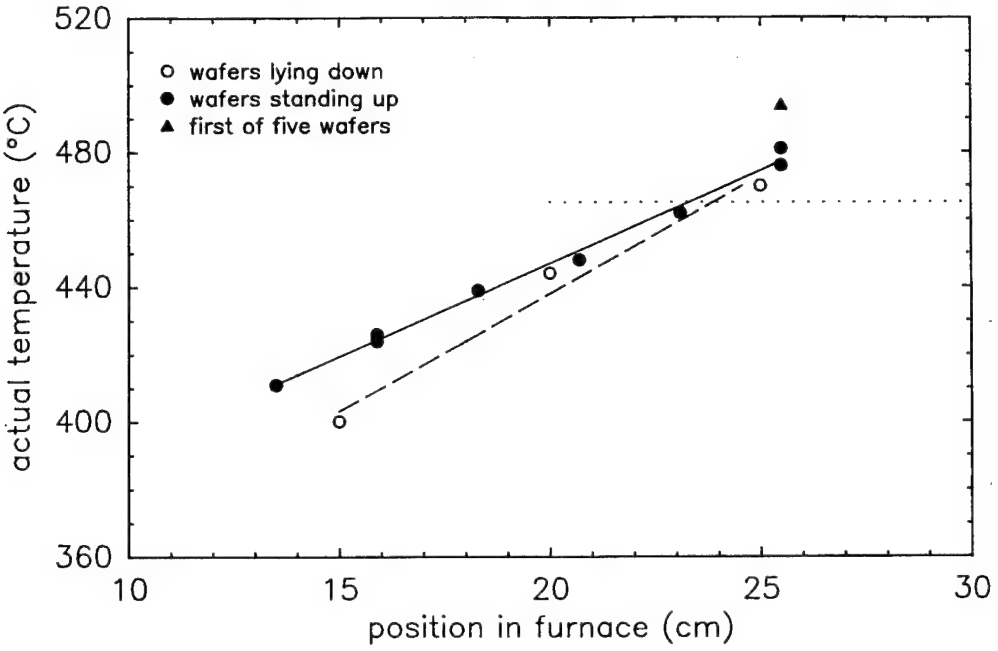


Figure 3-4 *Calibration of wafer temperatures in the vacuum furnace. These temperatures were measured with a thermocouple cemented to the wafer surface. The setpoint was 465°C.*

Table 3-6 *Back Contact Anneal Temperature.*

Alloy Temp. (°C)	Appearance	Electrical Resistance (1 mm mesa) (ohms)	Pull Strength (1 mm tab, 2 trials) (newtons)
		First Trial	
415	pink	3	not tested
425	pink	4	"
435	gray	4	"
445	gray	3	"
455	silver	2.5	"
465	silver	4	"
		Second Trial	
300	gold	non-ohmic	0, 0.2
350	gold	non-ohmic	0.7, 3.6
400	pink	ohmic	2.5, 1.8
425	gray	ohmic	1.4, 1.9
450	silver	ohmic	2.6, 5.8
475	silver	ohmic	1.1, 6.2

The physical properties of the contact metallization changed markedly as well. Before alloying, the film is very soft, and easily scratched off of the wafer. However, after alloying, even at a relatively low temperature, the AuZn film is quite hard and adherent to the surface; no lifting of properly alloyed back metallization was observed during this project.

Finally, the soldering of tabs to the back metallization of the cell was investigated. A number of test samples of InP with the normal Zn-Au back contact were made and annealed at various temperatures, from 350 to 475°C. Tabs 1 mm wide were soldered to each piece and pulled off, and the pull strength was measured. The I-V characteristics of the contacts were measured on other pieces which were prepared together with the pull test samples. It was found that all the contacts annealed at 400°C and above were ohmic and showed essentially the same contact resistance. Soldering was successful on all of these samples, with pull strengths ranging from 0.11 to 0.62 kgf. (1.1 to 6.1 N).

3.2.6 Front Contact Evaporation

The front contacts used in most of the cells made here were formed by evaporation through a photoresist mask, which was subsequently lifted off. The metal consisted of a thin layer of chromium (for adhesion), a thin layer of gold (to separate the chromium from the silver, and then a thick layer (about 5 microns) of silver. Silver was used because it has the highest electrical conductivity. A final layer of gold was added to facilitate interconnection (see Section 3.2.9).

The front contact evaporation procedure required considerable work during this project. In order to develop a process for the reproducible deposition of contacts with satisfactory adherence, it was necessary to experiment with the surface cleaning, and the evaporation temperature and rate.

Surface cleaning - The first of the technical problems concerning the front contact formation manifested itself as a separation of the metallization from the InP during the front contact sinter. Gas bubbles appeared under the metal in some places, and adhesion of the metal afterward was essentially nil, although the wafers would pass the tape test before sintering. We had never previously observed this phenomenon. By means of a series of experiments, contamination of the evaporation chamber and of the evaporation source was eliminated. It was found that InP wafers without photoresist did not suffer from this problem. Therefore, although silicon test wafers were not affected, it was concluded that contamination on the surface of the wafer was responsible. A number of cleaning procedures were tested in attempts to remove this hypothetical contamination, and one was found to be successful: exposure to oxygen plasma. In two cases, cleaned and uncleaned wafers were processed together, and the uncleaned wafers failed while the cleaned wafers showed no failure. The separation during the sinter has not recurred since the oxygen plasma was made a part of the process.

In the front contact work done at SERI, a similar observation was made, although in that case argon plasma was used. Specifically, a 30 KHz, 200 mtorr rf plasma was used to clean the photolithographically prepared surface just prior to metallization. The plasma exposure time was typically about 30 sec. It was determined that if this plasma pretreatment was used in conjunction with the stress-reducing deposition techniques described below, then the resultant adhesion was sufficient to support metallization up to 5 microns thick with line widths of 5 microns. These metallizations not only survived a scotch tape pull test, but also repeated scratching with a steel point (to simulate repeated mechanical probing). Although the materials studied were mostly oxide-coated InP, we believe that the same technique will give good results for InGaAs surfaces.

Stress and adhesion - The second problem, which arose immediately after the first problem was solved, involved the separation of the metallization from the InP before the sinter, during the liftoff process. Typically, most of the grid lines and pads would come off of the wafer, and those that remained would be easily removed by the tape test.

Contamination was again suspected, but another thorough cleaning of the equipment and a set of experiments with different procedures yielded no positive results. Substituting Ti-Pd-Ag layers for the Cr-Au-Ag produced no change. In an attempt to drive off water vapor or other volatile substances from the surface, we increased the wafer temperature to 90°C during the evaporation; this gave no improvement.

We found that thin layers (less than 0.5 micron) did not suffer from this poor adhesion; it arose only when larger amounts of silver were used. This led to the hypothesis that stress in the silver film was responsible for the failure. Accordingly, we added water cooling during the evaporation to keep the wafer temperature closer to room temperature (previously it had been allowed to rise with the heat from the evaporation to approximately 60°C). This was successful for some time, but the problem subsequently returned.

At this point, we carried out a thorough investigation of the effect of substrate temperature on the stress of the deposited silver film.

Using one-inch GaAs wafers, we performed a series of evaporations and measured the bow of the wafers before and after with a surface profilometer. From the change in the bow, we calculated the stress in the evaporated films.

Each evaporation was 400Å of Cr, followed by 5.9 microns of silver. The evaporation rate for the silver was held constant at 23-24 Å/sec.

The temperature of the wafers was controlled by turning the water to the cooling plate on and off during the evaporation, and by the way in which they were mounted to the surface of the cooling plate. Some wafers were mounted with vacuum grease, ensuring good thermal contact to the plate; temperatures as low as 7°C were reached in this way. Others were simply mounted flat to the plate, and others had a layer of photoresist on the back, providing some degree of insulation. A thermocouple was mounted on the back of one wafer with vacuum grease, and its output was monitored. In most of the runs, a bare wafer and a wafer with a resist-coated back were used as well.

Table 3-7 and Figure 3-5 show the results of this experiment. The data clearly show that temperatures significantly below room temperature lead to high stress in the silver. Although there is some indication of higher stress with increasing temperature above room temperature, there is too much scatter to make this conclusive.

As a result of this experiment, we established the following standard procedure, which appears to give consistent evaporation temperatures in the neighborhood of 25-35°C.

1. Coat the backs of all the wafers with photoresist.
2. Make sure the plate is at room temperature before loading the wafers.
3. Do not turn on the cooling water until the evaporation is started.
4. Do the evaporation all in one step; if it is necessary to stop for some reason, turn off the cooling water.
5. Turn off the cooling water as soon as the evaporation is finished.

Table 3-7 *Results of Stress Measurement in Silver Films.*

Wafer #	Back Surface	Evap. Temp.[a] (°C)	Bow Before evaporation[b] (microns)	Bow After evaporation[b] (microns)	Change in bow[b] (microns)	Stress[c] (10^9 dyne/cm^2)
1	TC	25	4.07	- 3.45	- 7.52	-1.24
2	bare	25	3.93	- 8.30	-12.23	-1.90
3	resist	25	4.88	- 2.60	- 7.48	-1.20
4	TC	35	5.05	- 5.17	-10.22	-1.64
5	bare	35	-0.60	- 5.52	- 4.92	-0.81
6	resist	35	1.79	- 0.62	- 2.41	-0.39
7	TC	72	6.40	0.89	- 5.51	-0.81
8	bare	15[d]	4.81	-13.43	-18.24	-2.80
9	resist	15[d]	4.25	- 0.74	- 4.99	-0.77
10	TC	45	1.61	- 6.97	- 8.58	-1.33
11	bare	45	0.55	- 5.03	- 5.58	-0.88
12	resist	45	1.15	- 7.81	- 8.96	-1.42
13	TC	15	-0.50	- 6.70	- 6.20	-0.98
14	TC	7	3.60	-11.40	-15.00	-2.38

[a]This is the temperature measured on the thermocouple wafer; the actual temperature of each wafer was not measured.

[b]The bow was measured on the front surface of the wafer; negative numbers indicate a concave front surface.

[c]Negative numbers indicate tensile stress.

[d]Estimated temperature.

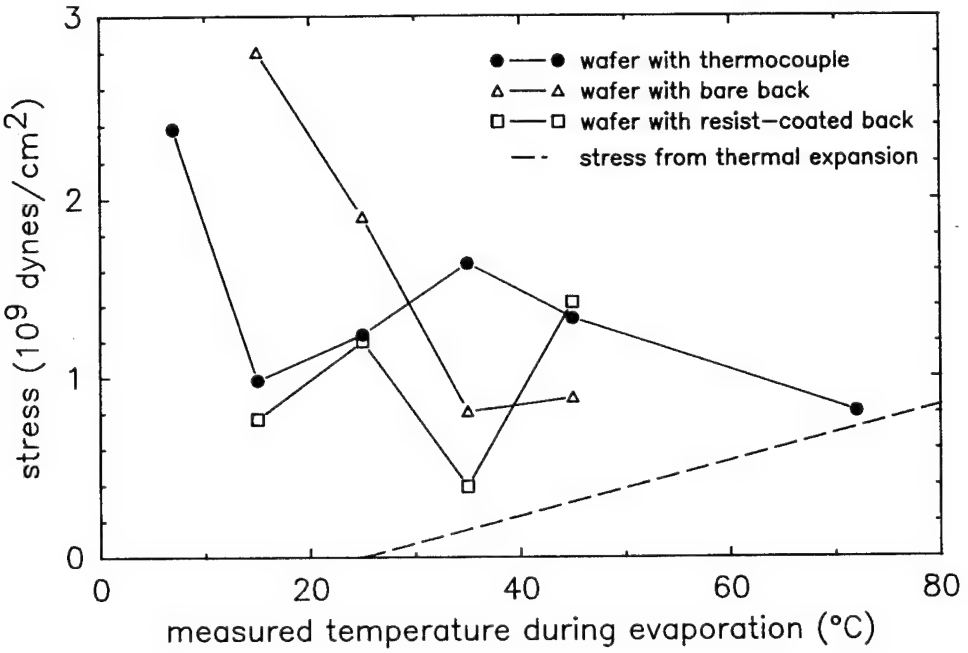


Figure 3-5 *Stress as a function of evaporation temperature in silver films. Stress increases if the wafer temperature is significantly below room temperature.*

Using this process, front metallization was quite consistent. In some cases isolated fingers or pads would be lost during liftoff, but the effect on cell performance and yield was small. Tape tests were conducted on some lots, and were successful.

At SERI also, similar conclusions were reached. It was found there that by increasing the deposition rate of the silver evaporation from 20 A/sec to 50 A/sec, the amount of stress in the silver was reduced (quantitative measurements were not made). It seems likely that the higher evaporation rate increased the sample temperature. (No cooling was used.) Although favorable results were not seen at the same evaporation rate at Spire, the finding that temperatures slightly above room temperature are beneficial appears to be general.

Problems have arisen occasionally with subsequent handling; on two occasions grid lines have come off of completed cells. In particular, grid lines came off of three Spire cells which were used for the UOSAT flight experiment, during mounting and covering at Spectrolab; the exact conditions which caused this are not known. Since cells made at SERI survived the same procedures, it appears that those cells have better adhesion than those made at Spire.

One possible explanation, which was suggested by SERI, is oxidation of the contact metal. The SERI cells used palladium as a diffusion barrier to protect the first layer of metal in contact with the InP. The Spire cells used gold, which, according to SERI research, is not as effective. Since the cells which were damaged at Spectrolab were exposed to air for a period of months before they were used, oxidation of the chromium is a possibility.

The discrepancy between the laboratory results and the results of handling outside of the laboratory underscore the need for a more quantitative test of contact adhesion than is currently available (the tape peel test). With no such test, it is not possible to establish standards or specifications for the grid adhesion, or to gauge the progress of any research aimed at improving it.

Some investigation of the interface and diffusion characteristics of the Au and Cr contact systems on InP was carried out at SERI using Auger spectroscopy and depth profiling. The results of Pd/Cr/InP contacts indicated that, even at room temperature, the Cr appeared to diffuse into the InP to a considerable depth. However, the Cr did not appear to penetrate much deeper as the annealing temperature increased. On the other hand, measurements of Au/InP contacts indicated that the Au did not diffuse as deeply into the InP during the room temperature deposition, but demonstrated more temperature dependence, diffusing to a greater depth after a 400°C anneal than the Pd/Cr/InP contact. It was speculated that the Cr forms a relatively stable oxide on the InP surface during Cr deposition. Unfortunately, a shortage of funds prevented the work at SERI from proceeding further.

3.2.7 Cap Etch Process

The use of the cap layer required the development of a new process: etching the cap layer off of the active area of the cell. The cap layer remains under the metal, but it must be removed from the rest of the cell because it will prevent the light from reaching the active regions.

Chemical etching was considered the simplest way of doing this. Since the cap is considerably thicker than the emitter (250 nm vs. 25), and the emitter thickness must be precisely controlled, a highly selective etch is essential to make sure of the complete removal of the cap without affecting the emitter thickness. Other potential problems include reactions between the etching solution and the metallization, and undercutting of the etch (removal of the cap layer under the metal from the side.

At first, we followed the work of Choi *et al.*,[16] using a sulfuric acid-peroxide-water etch at low temperature. The selectivity was tested by measuring etch rates on dummy InP wafers and found to be excellent; no measurable etching was observed. Silver films were exposed to the etch as well; they showed some discoloration but no measurable change in thickness.

The first cells with cap layers were etched using this solution. About 15 seconds was found to be necessary for complete removal of the cap layer; the endpoint was easily determined with the naked eye. Results of the cell measurements (Table 3-5 above) showed that the etching was complete and had not had any other adverse effect on the cell. One of the cells was deliberately overetched (etched for an extra 4 minutes) and retested; its performance did not change significantly.

This gave us a satisfactory etch, which was used for several lots of cells. After the first lots, a thin layer of gold was added at the top of the front metallization to protect the silver; this prevented the discoloration.

Although this etch was entirely satisfactory from a laboratory point of view, it was felt that a solution which could be used at room temperature and did not require sulfuric acid would be preferable for production. Accordingly, another formula reported in the literature was tried: a phosphoric acid--peroxide- water mixture. Results with this solution were very similar, and so it replaced the sulfuric-based etch in the standard process.

Undercutting of the cap layer has proved to be a problem only in a few cases in which the cap composition was not correct. Normally, the etch rate is about 1 micron per minute, and only 15-30 seconds is required to remove the cap. Thus, the amount of undercutting should be only 0.5 microns on each side of the grid lines (assuming isotropic etching). Since the grid line width is 10 microns, this does not impair the grid line adhesion or conductivity.

3.2.8 Antireflection Coating

Optical coatings for these cells were done with vacuum evaporation. At first, only resistive heating was used, because experience with GaAs and silicon indicates that some damage to the cell results from stray radiation during electron beam evaporation. However, electron beam evaporation was tested on some cells and no degradation was observed, so it was incorporated into the process; this enabled us to use Al_2O_3.

Two coatings were developed: one for optimum performance without a cover and one for optimum performance with a cover. Since the refractive indices of the coverglass and adhesive affect the reflectance at the cell surface, different coatings must be used.

In both cases, two-layer coatings were found to be beneficial. For the uncovered cell, the best combination of available materials was ZnS/MgF_2, and for the covered cell it was ZnS/Al_2O_3. For the ZnS and MgF_2, which were deposited with resistive heating, the thickness was controlled by controlling the weight of the source material (the source was completely evaporated). With the ZnS in particular, the crystal monitor was found to give inconsistent results. With the Al_2O_3, electron beam heating was used, and the thickness was controlled with a crystal monitor.

The measured and calculated spectral reflectance of these coatings are shown in Figure 3-6 for the uncovered cell and Figure 3-7 for the covered cell. Table 3-8 gives the weighted integral of the reflectance for these two cases and for intermediate stages of the cell process. The reflectance of the coverglass front surface was assumed to be 0.013.

These measured values are expected to be about 2% higher than the theoretical values because they include the reflectance of the metal grid lines. As Table 3-8 shows, the best coating with a cover is not as good as the best coating without a cover, so the final efficiency of the covered cell will be correspondingly less than the values measured in the laboratory with no cover. The single layer, however, shows lower reflectance with the cover; thus, the advantage of using a double layer is less in the covered case.

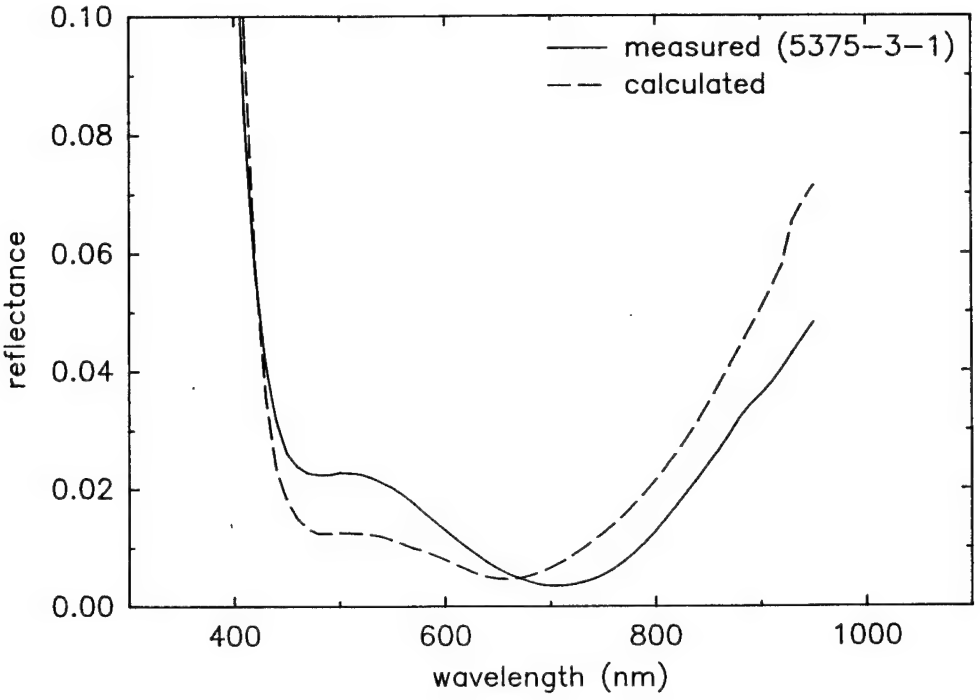


Figure 3-6 *Measured and calculated reflectance of an uncovered cell. The integrated reflectance is 3-4%.*

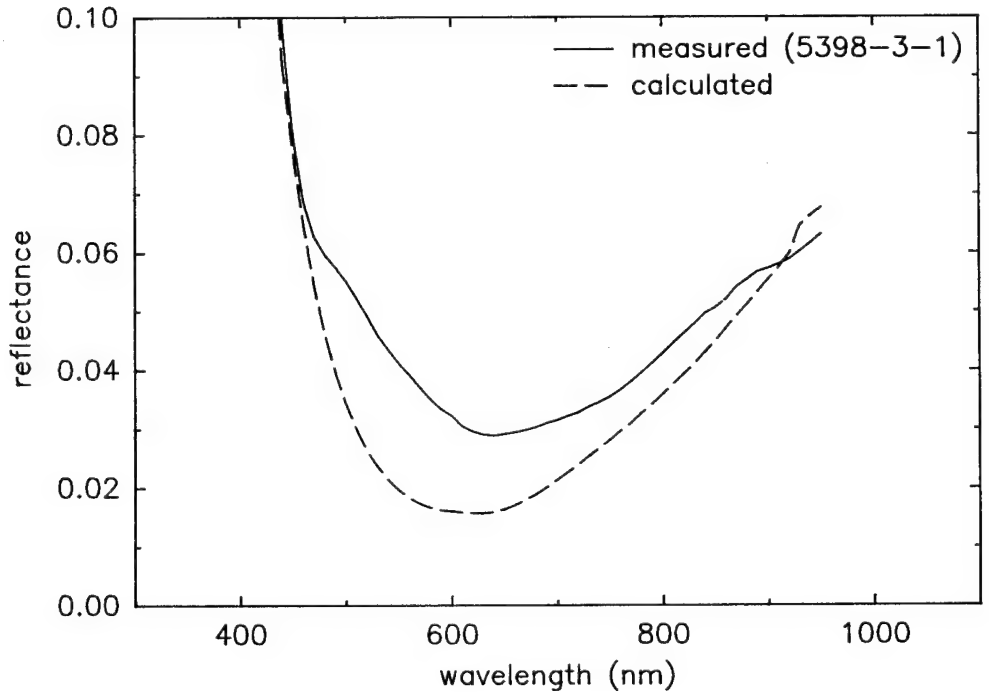


Figure 3-7 *Measured and calculated reflectance of a cell with a coverglass. The integrated reflectance is about 5%.*

Table 3-8 Measured and Calculated Reflectance of InP Cells.

Cell Structure	Measured R	Calculated R
Bare InP surface	n.m.	0.323
InP/ZnS/air (single layer AR)	0.11	0.108
InP/ZnS/MgF_2/air (double layer AR)	0.035-0.04	0.031
InP/ZnS/Al_2O_3/air (double layer AR)	0.04-0.06	0.043
InP/ZnS/adhesive (single layer w/cover)	0.07	0.085
InP/ZnS/Al_2O_3/adhesive (double layer w/cover)	0.05	0.048

Because of the need for bonded contacts, it was also necessary to develop a process to remove the coating from the metallized area of the cell. This was done by using a photolithographic mask and etching the Al_2O_3 and ZnS with concentrated hydrofluoric acid.

It should be noted that, despite several attempts, we were not successful in finding a corresponding etch for the MgF_2, so the MgF_2/ZnS coated cells could not be bonded. Another problem with the MgF_2 was its tendency to come off of the cell surface during the sawing process; no such problem arose with the Al_2O_3.

3.2.9 Bonding of Interconnect Ribbons

Another goal of this project was the development of interconnection processes for these cells. A method of attaching metal leads to the cells reliably with reasonable strength and stability and without damaging the cell itself is essential.

To facilitate this work, a special mask was designed and obtained with a large number of contact pads of three sizes (1 mm square, 1 x 1.5 mm, and 1 x 2 mm). When used with the same lithography and metallization processes as are used to make the cells, this mask provides many contact pads identical to those on the cells themselves which can be used for testing contact processes. Pull strengths were measured by clamping the free end of the ribbon to a Chatillon digital force gage and pulling manually at a 45° angle to the surface until the ribbon came off of the surface.

Soldering - Since soldering is the most common and simplest process for attaching contacts, it was tried first. Using standard tin-lead-silver solder (Sn62/Pb36/Ag2) and flux (Kester type R), copper ribbons were attached to the 1 mm^2 silver contact pads and pull tests were carried out.

The first results were not successful. One sample had a pull strength of 0.9 N, but most were less than 0.1 N. Soldering was tried with and without solder preforms, but results were unsatisfactory in both cases. Somewhat better results were obtained with the larger pads.

Examination of the failed samples showed that the tab had removed a considerable piece of InP as well as the metallization; thus, the failure was not in the metallization or the solder itself. Further examination showed that the solder had covered part of the edge of the pad. When soldering was repeated, using careful procedure to confine the molten solder to the metal pad surface, much better results were achieved. Pull strengths up to 5.6 N were measured on 1 mm^2 pads under these conditions; in many cases, the wafer broke before the tab was removed.

From these observations, we can draw the hypothesis that contact with the molten solder physically damages the InP. If the solder is kept on the metal surface, the silver prevents this damage, but where the liquid metal touches the edge of the pad, it contacts the InP itself, and some reaction presumably takes place which seriously weakens the material, leading to failure of the contact pad.

Despite the relatively good results achieved once this problem was recognized, we were not successful in making the process reliable. On the last trial, seven out of 16 bonds had strengths less than 0.1 N; the other nine ranged from 1.8 N to 6.3 N.

An attempt was made to use parallel-gap soldering (in which the heat is supplied electrically, rather than with an iron), but this led to greater damage to the InP, apparently from thermal shock.

Thermosonic bonding - To avoid these problems, we turned to thermosonic bonding. Not only does this involve no liquid metals, but it requires no flux, thus making the process simpler and eliminating concerns about corrosion by the flux.

In the bonding experiments, gold and silver contacts were compared; gold is generally more amenable to bonding because it is softer. Some wafers were made using 5 microns of silver with only 20 nm of gold on the top, others with 4.5 microns of silver and 0.5 microns of gold, and other with 5 microns of gold. At the same time, normal evaporated contacts and contacts made by sputtering the first layer were compared. Dummy InP wafers with a layer of InGaAs (to simulate the cell structure) were used, along with GaAs dummy wafers for controls.

The bonding work required considerable adjustment of the parameters: temperature, ultrasonic power and time, and pressure. A special fixture was designed and built to hold the cells. Bonding near the edge of the pad, or using a wedge which was worn or otherwise out of the correct shape, was found to be detrimental to forming a good bond.

Once the process was satisfactorily developed, we found that either gold or silver ribbons could be bonded consistently to gold pads, but bonding silver ribbons to silver pads gave less reliable results. Attempts were also made with silver-coated molybdenum ribbons, but these were unsuccessful; the stiffness of the ribbon interfered with the formation of a good bond.

Pull strengths were found to range from 0.2 N to 1.5 N for a 1 mm pad under the optimum conditions. Although we found some evidence that the sputtered metallization gave better results than the evaporated metallization, this was not conclusive. Testing of cells before and after bonding showed that the series resistance of the contact was low and that there was no measurable degradation of the cell efficiency associated with the bonding process.

3.2.10 Coverglass Application

Although the coverglass application appears to present no new difficulties in the case of InP, it was necessary to cover some cells and verify the proper functioning of the process.

For this project, it was expected that the thickness of the contact ribbon on the front of the cell might present a problem for the covering, so covers were made to cover all of the cell except one mm of the edge with the contact pads. It was subsequently found that this was unnecessary; the pads and ribbons can be easily covered as well, but all the cells in this program were covered in this way.

In accordance with NRL requirements, fused silica of 6 mil and 12 mil thicknesses, with antireflection and UV rejection coatings, were used.

Coverglass application was carried out manually. Dow- Corning 93-500 space-grade adhesive was de-aired in a vacuum, a measured amount was applied to the center of the cell, and the coverglass was placed on top. When a weight was carefully applied to the surface, the adhesive formed a continuous, even film. Small bubbles occasionally formed, but none larger than about 1 mm. The adhesive was cured by baking the assembly in an oven, with the weight in place. The measurements reported in Table 3-8 indicates that the reflectance of the covered cell is as expected and there was no unexpected loss of cell performance resulting from the covering process.

3.2.11 Back Contact Soldering

We have considerably more latitude in making contact to the back of the wafer than to the front, since the back is completely covered with metal, and there is no need to be concerned about shadowing losses. We achieved satisfactory results with soldering, and so decided to use that, rather than developing a process for thermosonic bonding, which would probably require a substantially greater metal thickness.

Since the properties of the intermetallic gold-indium-zinc compound formed at the back surface by the alloying process are not very well known, we originally covered it with an 0.5 micron layer of silver. This layer, evaporated after the alloying step, was intended to give a better contact both in testing (in which the cells are held on a flat surface by a vacuum), and with the soldered contact. In some cases, though, the silver layer showed poor adhesion, so for reasons of reliability and simplicity it was desired to do without it.

For this development work, ribbons were soldered to the backs of test wafers and pulled, similarly to the front contacts described above. Using the simple technique of dipping the pre-tinned ribbon into a non-corrosive flux (Xersin #2112) and soldering to the surface with an iron, we found better results without the silver overlayer than with it. In a group of 18 tests with 1 mm wide tabs, all but two had 2 N or more of pull strength, and in 12 of the cases, the ribbon or the wafer broke before the bond itself.

3.2.12 Panel Assembly

As required under the contract, two panels of 20 cells each were assembled from cells made here. One graphite substrate and one aluminum substrate were used. Terminals and temperature sensors were installed in accordance with the directions of NRL; Figure 3-8 shows a mechanical drawing of the design, and Figure 3-9 shows a photograph of one completed panel.

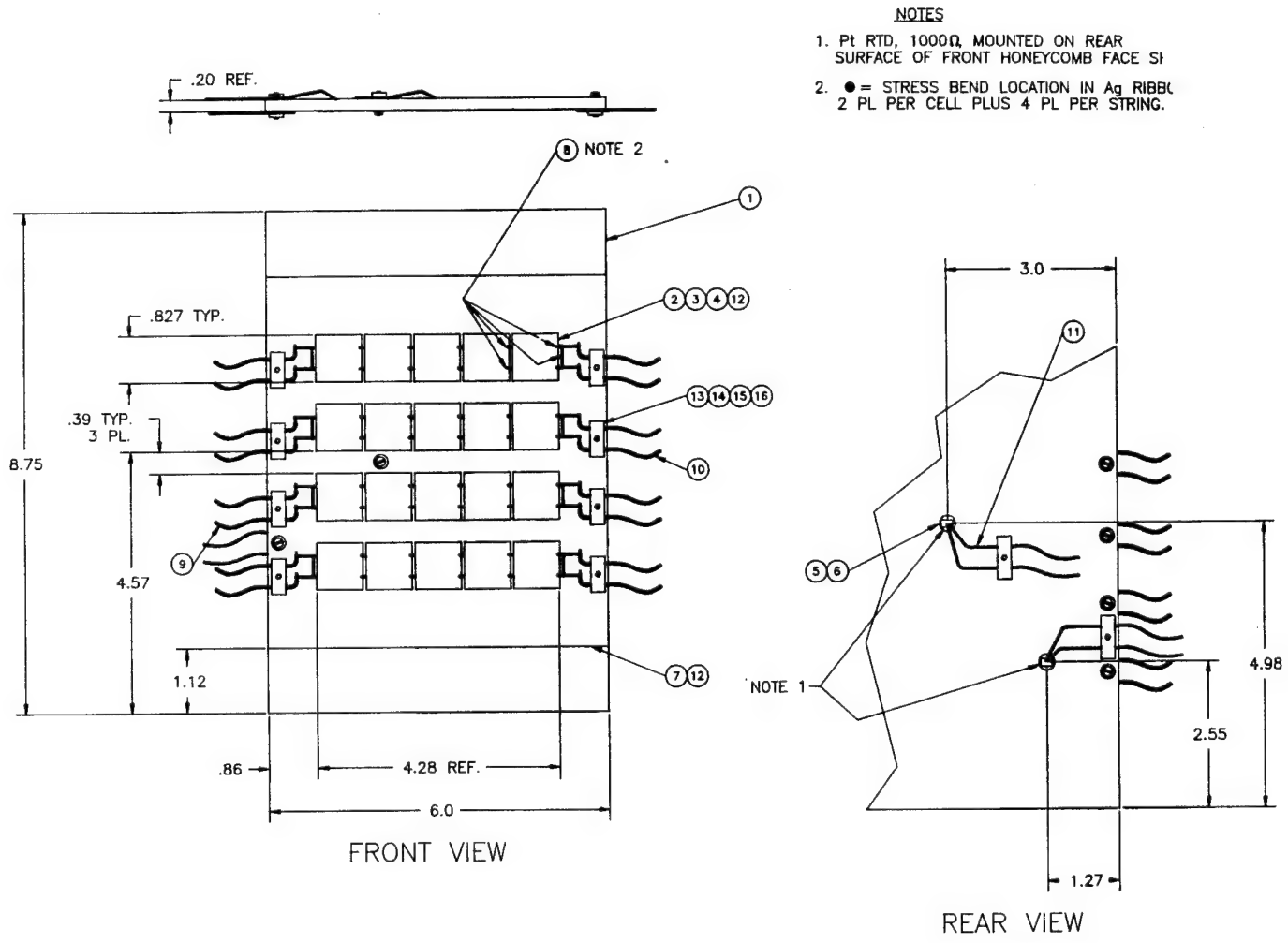


Figure 3-8 *Design of InP solar cell panel. Four strings of five solar cells are mounted on the panel and wired independently.*

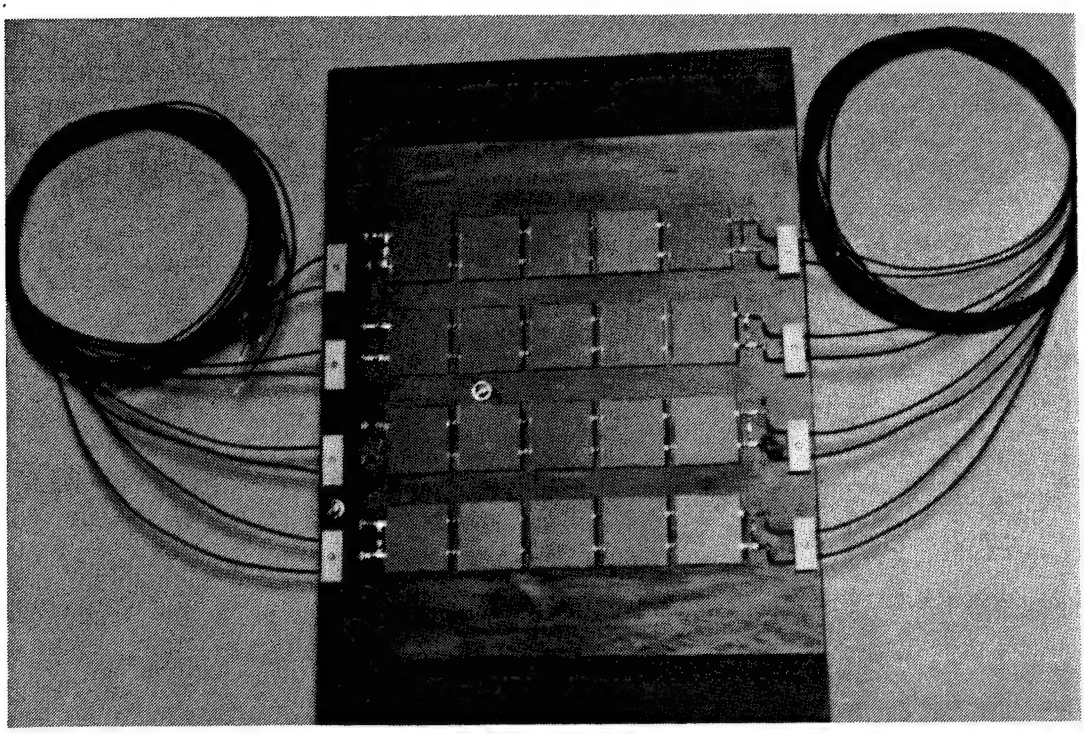


Figure 3-9 *Photograph of completed panel. The two temperature sensors are also visible, near the center and toward the left edge.*

Each panel had four strings of five cells, which were connected in series. The ribbons from the front of each cell were soldered to the back of the next cell, after bends were made to prevent stress from arising from the thermal expansion mismatch. Each of the four strings had four leads, two from the positive end and two from the negative end, which were soldered to free wires; there was no connection among the strings.

A layer of FR-5 epoxy-impregnated fiberglass cloth was mounted on the substrate surface for insulation, and the cells were mounted on the cloth. McGhan NuSil CV-2568 low-volatility silicone adhesive was used for both of these joints. Before making the panels, the peel strength of this adhesive was measured on test pieces and found to be 0.6 pounds per inch on the substrates and 1.1 pounds per inch on the cell back surface, when used with the McGhan NuSil SP-120 primer. (Strength was much lower without the primer.) This was considered acceptable.

After assembly, one cell was broken by a mishap, and two others were discovered to have small cracks; these cells were replaced by carefully removing the broken cell from the string, mounting another in its place, and making solder connections between the ribbons.

The panels were tested after final assembly, and the results compared to those from the same cells before assembly. Results are shown in Table 4-6 of Section 4.4.

3.3. DETAILED DESCRIPTION OF THE CURRENT PROCESS

The following is a detailed description of the standard process which is the result of the development efforts described above in Section 3.2.

3.3.1 MOCVD Growth

MOCVD growth begins with InP wafers, diameter 50-56 mm, zinc doped to 2×10^{18} cm^{-2} or greater, with etch pit density of 10^5 cm^{-2} or less, orientation 2° off (100) toward nearest (110), polished on one side.

The surface polish is crucial to good results; the surface must be free of crystal damage which can result from the polishing process and is not visible to the eye before growth. Our experience has shown that some vendors can supply wafers which consistently give good results without any cleaning or etching procedures before the growth.

The wafers are loaded into the MOCVD reactor to begin the growth process. The general characteristics of the reactor are given in Table 3-9.

Table 3-9 *SPI-MO CVD™ 450 General Characteristics.*

Geometry	Vertical Gas Flow, Frustum Susceptor
Capacity	5 wafers, 56 mm dia.
Main Gas Flow	5 lpm Pd-diffused H_2
Chamber Pressure	1 atm.
Susceptor Temperature	600°C
In source:	ethyldimethylindium bubbler, 17°C (0.85 torr)
P source:	100% PH_3
Ga source:	trimethylgallium bubbler, 0°C (68 torr)
As source:	100% AsH_3
Zn source:	dimethylzinc in H_2 100 ppm with dilution line
Si source:	silane in H_2, 20 or 500 ppm

The growth process itself consists of a heating step, five growth steps, and a cooling step. Table 3-10 gives the parameters used in each of these steps. The flowrates for each reactant are given in standard cubic centimeters per minute, and the numbers in parentheses are the calculated mole fractions of each component in the total gas flow.

Table 3-10 *Growth Process for InP Solar Cells. (Figures in parentheses are mole fractions of the total gas flow).*

Step	Time (s)	In Flow	Ga Flow	P Flow	As Flow	Si Flow	Zn Flow
1. Heat up				60 sccm (0.012)			
2. Buffer	1000	300 sccm (6.7×10^{-5})		60 sccm (0.012)			40 sccm (8×10^{-7})
3. Base	6000	300 sccm (6.7×10^{-5})		60 sccm (0.012)			0.2 sccm (4×10^{-9})
4. Emitter	130	150 sccm (3.4×10^{-5})		60 sccm (0.012)		112 sccm (4.5×10^{-7})	
5. Emitter	70	150 sccm 3.4×10^{-5})		60 sccm (0.012)		30 sccm (3×10^{-6})	
6. Cap	60	300 sccm (6.7×10^{-5})	5 sccm (8.9×10^{-5})		200 sccm (0.04)	200 sccm (2×10^{-5})	
7. Cap	224	300 sccm 6.7×10^{-5})	5 sccm (8.9×10^{-5})		30 sccm (0.006)	200 sccm (2×10^{-5})	
8. Cooling					30 sccm (0.006)		

After the growth process is completed, the wafers are inspected optically to verify that no contamination or crystal damage has interfered with the growth. Test pieces are cut from a wafer and the following measurements are done to measure the critical parameters of the growth.

1. Etching - A piece is etched in the cap etch (See section 3.3.2 below). This allows measurement of the cap thickness (by surface profilometer).

2. Van der Pauw - Performed on a piece with the cap layer removed, this determines the sheet resistance and sheet carrier concentration of the emitter layer. The goal is 200-500 ohms and 1-3 x 10^{13} cm^{-2}.

3. C-V profiling - Performed with an electrochemical C-V profiler, this determines the thickness and carrier concentration of the p-type base layer. The goal is 3 microns and 5-15 x 10^{16} cm^{-3}. The cap and emitter layers must be removed by etching first, because the heavily-doped emitter interferes with the measurement.

4. Groove and stain - Performed on a GaAs test wafer, this measurement gives the total thickness of the InP layers, and is used to calibrate the growth rate.

3.3.2 Cell Processing

Processing of the MOCVD-grown wafers begins with the back contact formation. First, photoresist is applied to the front of the cell and baked. The back surface is then etched, first with a cap etch and then with HCl, to remove any deposit of InGaAs or n-type InP that might have formed on the back of the wafer during the MOCVD growth and to provide a clean surface for the back contact. The resist is then removed with acetone and the wafers are placed into the evaporator for back metallization.

A mixture of 95% gold with 5% zinc is used as the source material. The amount needed to give approximately 100 nm of metal thickness (250 mg in our system) is loaded into the Mo boat. The wafers are loaded with silicon dummy wafers covering the fronts, to prevent the deposit of metal on the front. The chamber is evacuated to 2×10^{-6} torr and the boat heated carefully until empty. The evaporation rate is monitored with a crystal thickness monitor, and the power is controlled to keep the rate in the neighborhood of 1 A/s.

The alloying step is carried out after the wafers are removed from the evaporator; no other steps intervene. The wafers are loaded on a boat in a 3-inch quartz tube which is mounted next to a furnace. A gold-coated silicon wafer is mounted at the outer end of the tube to reduce heat loss by radiation and make the temperature more uniform. The tube is sealed and evacuated to 5×10^{-6} torr, while the furnace is heated and stabilized at 420°C. Then the tube is moved into the furnace for 7 minutes. The furnace temperature, as indicated by the thermocouple outside of the tube, drops at first, then rises again, reaching about 410-415°C at the end of the seven minutes. At this point, the tube is removed from the furnace and allowed to cool, then to return to atmospheric pressure. The wafers are removed and inspected; a gray or silver color of the back surface indicates that the alloying step was successful.

At this point, the wafers are ready for front contact photolithography. Resist is applied to the front surface and baked. Then the grid pattern is exposed through a mask using a contact aligner. Figure 3-10 shows the pattern used in this mask for the 4 cm^2 cell. This mask has transparent grid lines on an opaque background; the image is reversed from what would be used in a simple liftoff process.

The exposed wafers, without being developed, are then baked for one hour at 90°C in a vacuum oven under an atmosphere of anhydrous ammonia. This step acts to reverse the image by rendering the previously exposed areas insensitive to development. After the wafers are removed from this oven, they are exposed to UV light again, covering the entire surface, then developed. This way, the parts which were masked during the first exposure are developed, and the exposed parts (the grid lines) are not.

Doing the exposure in this way allows the grid line pattern to be defined with an undercut profile, which facilitates liftoff of thick evaporated films (Figure 3-11).

A layer of photoresist is painted on the backs of the wafers and baked, to provide thermal insulation during the evaporation (see Section 3.2.6). The front grid pattern is inspected with a microscope to verify that the lines are continuous and have the desired width.

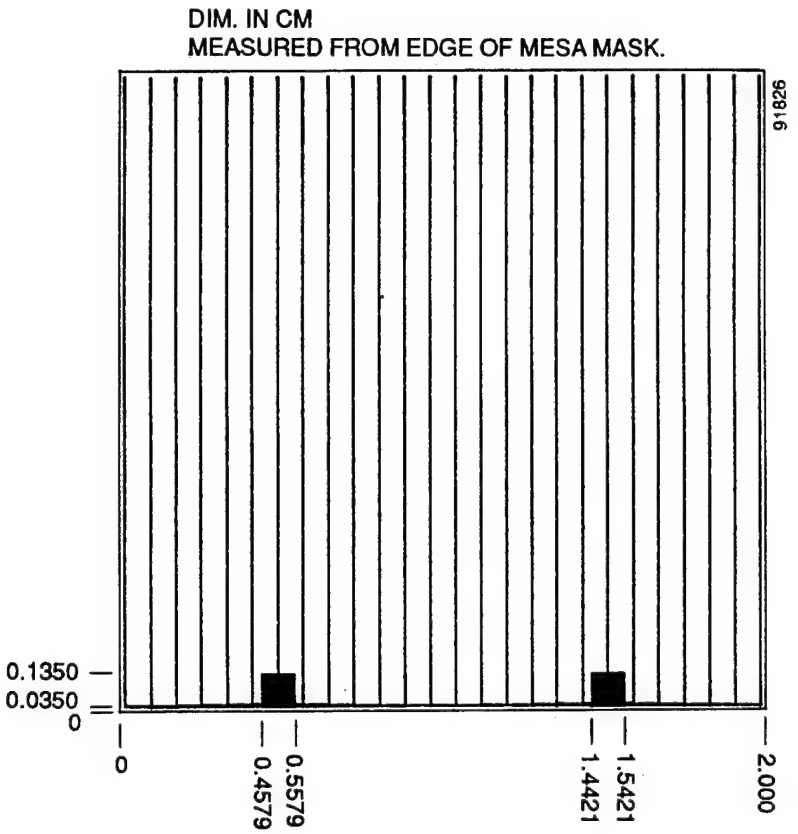


Figure 3-10 *Mask pattern for 4 cm^2 cells. The pattern has two contact pads, each 1 mm^2, and 26 grid lines, each 10 microns wide.*

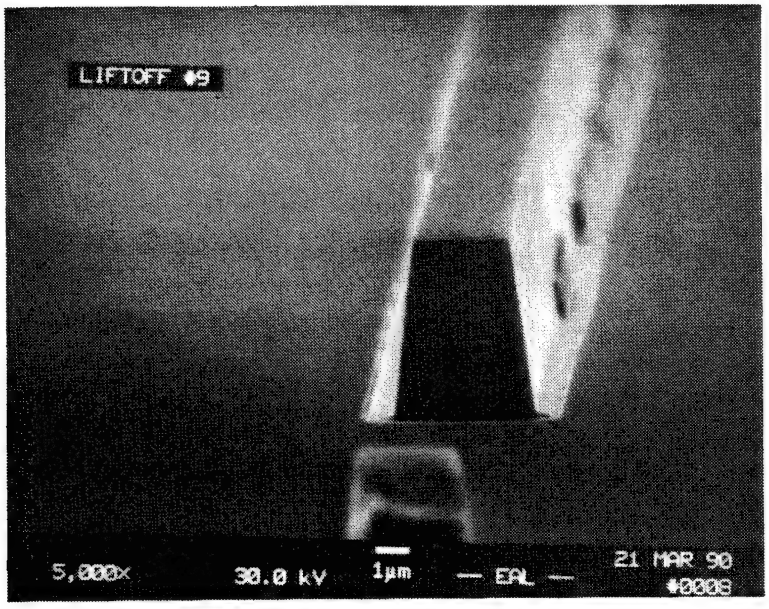


Figure 3-11 *SEM photo of grid lines formed by evaporation and liftoff. The height of the lines is 5 microns.*

Shortly before evaporation (within 4 hours), the wafers are dipped in a solution of 10% NH_4OH in water for 10 seconds to remove any remaining resist residue. They are then exposed to an oxygen plasma for 6 seconds in a plasma etcher which generates 250 Watts of rf power, and finally dipped in buffered HF solution for another 10 seconds, rinsed, and dried. The wafers are loaded onto the water-cooled plate in the electron-beam evaporator, observing the procedure described in Section 3.2.6 to maintain the temperature at or slightly above room temperature during the evaporation. Four evaporations are done sequentially, without opening the chamber: 40 nm of Cr, 40 nm of Au, 4.7 μm of Ag, and 30 nm of Au. The evaporation rate is 2 nm/s for the silver.

The wafers are inspected by eye both during and after the evaporation for any peeling of the metal films, which is a sign of excessive stress. A dummy wafer is also included with the batch, which allows the total metal thickness to be measured with a profilometer.

After removal from the evaporator, the wafers are soaked in acetone to remove the excess metal. This usually takes about two hours; the metal then separates from the surface as a continuous foil. Agitation is not needed. The wafers are then rinsed in more acetone and methanol, dried, and carefully inspected for missing fingers or other metal areas in which the adhesion has failed.

Next, the wafers are prepared for the mesa etch. Again photoresist is applied and baked. A mask with opaque squares defining the active areas of the cells is used for the exposure; exposure and development are done normally. Resist is applied to the backs and baked.

The next step uses an InGaAs cap etch and an HCl etch. The InGaAs etch (described in Section 3.2.7) is phosphoric acid, hydrogen peroxide, and water in 1:1:8 proportions; this etches InGaAs at about 1 micron/minute and has no measurable etch rate on InP. The InP etch is straight 12 N HCl, and etches InP at about 5 microns/minute.

The wafers with the photoresist pattern are etched first in the InGaAs etch to remove the cap layer. Because InP and InGaAs have a noticeably different color, the endpoint of this etch can be observed by eye; for a 250 nm cap it usually takes about 15 seconds. Next, the wafers are etched in the InP etch to form the mesas. Since it is only necessary to remove the thin (30 nm) emitter, ten seconds of etching is easily sufficient. This allows the progress to be checked as well, because the InP will produce gas bubbles in the etch, but if the InGaAs removal is not complete, visible bubbles will not form.

After the mesas are formed, the resist is removed from these wafers, exposing the active area, which is still covered by the cap. The cap is now removed from this area by etching again in the InGaAs etch, and observing the cell areas to see the endpoint. When the etch is complete, the wafers are rinsed and dried.

At this point, the cells are fully functional, although the lack of an antireflection coating reduces their efficiency. For research purposes, the cells are usually tested here and the efficiencies recorded.

Next, the antireflection coating is applied. The wafers are loaded into the thermal evaporator, along with a blank InP test chip, and 165 mg of ZnS is placed in the Ta boat. After evacuating to 2 x 10^{-6} torr, the ZnS is carefully heated to evaporation. The rate is controlled with the crystal monitor and the heat is adjusted to keep it at about 2-3 Å/s. The evaporation is continued until the boat is empty. The chamber is opened and the film thickness on the test chip measured with an ellipsometer; the target is 600 $\pm$ 50 Å, and the refractive index is normally 2.33.

Next, the wafers are loaded into an electron beam evaporator for the Al_2O_3 coating. The evaporation is performed with Al_2O_3 pieces in an atmosphere of about 10^{-4} torr of pure oxygen. In this case, the previously calibrated crystal monitor is used to determine the endpoint, although a test chip is still checked afterward. The target thickness is 800 $\pm$ 100 Å, and the refractive index is normally about 1.56.

This coating must be removed from the contact pads for best results in testing and bonding. This is also done with photolithography. Photoresist is applied and exposed as before, using a mask which covers most of the wafer and exposes only the contact pads. Photoresist is again applied on the backs as well.

The wafers are etched in buffered HF to remove the Al_2O_3 (about 90 seconds) and then in 6N HCl (1 HCl:1H_2O) to remove the ZnS (about 20 seconds). The HCl will attack InP slightly, but if photolithography is done carefully this can be avoided, since etching is only done on the metal-covered areas.

After the resist is removed, the cells are completed and can be tested. These five tests are routinely carried out; others may be used where appropriate:

1. All cells are tested for electrical output under the AM0 solar simulator. Complete IV curves are recorded.

2. Selected cells are tested for spectral response and reflectance, which allows calculation of the internal quantum efficiency.

3. Log I-V measurements are carried out on selected cells. Both dark I-V and I_{sc}-V_{oc} curves are measured and plotted.

4. A transmission line measurement is made on selected wafers, using a pattern placed next to the cells. The measurement gives the contact resistance and sheet resistance of the emitter layer.

5. Zero-bias capacitance is measured on other test pads on the wafers; this gives a measurement of the base doping density.

Finally, the wafers are sawed into cells. The pattern used throughout this project has two cells on each wafer; this was used with both 50 mm and 56 mm wafers. (In the future, it may be possible to make three cells from a 56 mm wafer.) Before sawing, the front of the wafer was covered with photoresist to protect the front metal, and the individual cells were numbered on the backs with a pencil. Plastic tape was then applied to the back of the wafer.

Plastic tape was found to be necessary to hold the pieces of the wafer together during sawing. Afterward, the cells and edge pieces are carefully peeled from the tape. Since it is not possible to avoid a certain amount of scraping together of the cut edges while peeling the tape, this is one area in which further work is probably needed. At first, we attempted to cut without the tape, cutting only part of the wafer thickness and breaking the rest after removing it from the saw. This method was found to be risky, however: in some cases the wafer broke while still on the saw, and cells were lost.

The sawing itself is done by an automatic dicing saw, using a 1.0 mil diamond blade, turning at 30000 RPM and moving at 0.12 cm/sec. Five cuts are needed to remove the two cells from the wafer.

After sawing, the cells are washed in acetone to remove the photoresist. After this point, the cells are handled by their edges only; before sawing, the wafer could be easily handled with tweezers by the inactive areas near the edges, but the sawn cell has no inactive areas, and is very sensitive to surface damage.

3.3.3 Panel Fabrication

Assembling a panel from these cells consists of four steps: bonding front contacts, attaching a coverglass, connecting the cells into strings, and fastening the strings to the substrate.

Front contact bonding is done using a thermosonic welder with a wedge-shaped bonding tool and pre-formed 0.001" x 0.031" silver ribbon. A semicircular bend is made in each ribbon before bonding, using a specially designed jig, to allow slack for thermal expansion mismatch. Bonding parameters are given in Table 3-11. Two bonds are made on each pad, taking care not to bond at the edge of the pad.

Table 3-11 *Bonding Parameters.*

Cell Temperature	140°C
Bonding Force	75 g
Ultrasonic Power	setting 8.2
Bonding Time	setting 8.5
Bonding Wedge Width	0.032 in.

After bonding, the coverglasses are fastened to the cells. First, the back of the cell is covered with Kapton tape to protect it from the silicone adhesive. The adhesive (Dow-Corning 93-500 Space Grade Encapsulant) is mixed according to the manufacturers instructions and de-aired in a vacuum chamber. Three drops of adhesive are placed in the center of each cell, and then the coverglasses are placed on top and carefully pressed down so that the adhesive covers the entire surface. The cells are cured (4 hours at 65°C) with a weight on top of the glass, and then the tape is removed from the back and the excess adhesive is cleaned off of the front of the cell with a razor blade and with methanol.

The assembly of a string is relatively straightforward. The free ends of the tabs of each cell are dipped in flux (Xersin #2112), dipped in solder (36% Pb:62% Sn:2% Ag), then dipped in flux again. The cells are placed face down in a specially designed holder that positions them with 2 mm of space between, and the free ends of each ribbon are allowed to rest on the back of the next cell in the string. The solder joints are made with a 700°F (371°C) iron. For this work, the joints were made toward the edge of the cell away from the previous cell, so that the free segment of ribbon is relatively long; this is to minimize deformation of the ribbon due to thermal expansion.

The final panel assembly consists of covering the substrate with the insulating fiberglass-epoxy sheet (using McGhan NuSil SP-120 primer and CV-2568 adhesive), and then attaching the completed string to the cloth (in the same manner). The adhesive was mixed and cured following the manufacturer's directions, which include curing for 7 days at room temperature.

The silver leads and the ends of the string were soldered to 24 AWG Teflon insulated copper wires and clamped into place to provide strain relief; more elaborate development of the interconnection scheme was not within the scope of the contract.

SECTION 4
CELL RESULTS

4.1 TESTING PROCEDURES AND CONDITIONS

All cells made in the course of this project were tested under simulated AM0 illumination for cell performance. A Spectrolab X-25 simulator was used. The simulator was calibrated before the measurement with a GaAs reference cell (Spire designation ST-17), which was calibrated at the Solar Energy Research Institute in March of 1989. Toward the end of the contract, a NASA-calibrated InP reference cell became available; the final measurements for panel fabrication were corrected using that cell, although measurements using ST-17 were still made in order to provide continuity through the project.

The cells were mounted on a temperature-controlled test block and held with vacuum. Five contacts were made: voltage was measured between a point contact on the back and a probe on one of the front pads, and current was measured between the test block itself and two probes on the front, one on each pad. Measurements were made with a 12-bit ADC, and full I-V curves were recorded for each cell.

4.2 RESULTS OF EXPERIMENTS

This section will report the results of the experiments and modeling that were done to explore the effect of the cell parameters on the performance.

4.2.1 Emitter Thickness

As mentioned in Section 3.2.1, the emitter thickness is the parameter to which the performance shows the greatest sensitivity. Figure 4-1 shows this effect, showing the quantum efficiency in the blue end of the spectrum for a cell as it is repeatedly anodized and its thickness decreases. Curves for a graded cell and an implanted cell are also shown for comparison.

After the process for producing the graded emitter was established, a final adjustment was made in the emitter thickness. Table 4-1 shows the growth runs made and the results obtained; by reducing the growth time for the last emitter layer from 100 s to 70 s, a further improvement in blue response and efficiency was found. Although the resulting sheet resistance increased somewhat, this proved not to be a serious problem.

The effect of thickness, and the progress which has been made in that area, is shown graphically in Figure 2-5. Spectral response curves are shown for three epitaxial cells, ranging from the first efforts at Spire, in which the emitter thickness was 300 nm, to the present results.

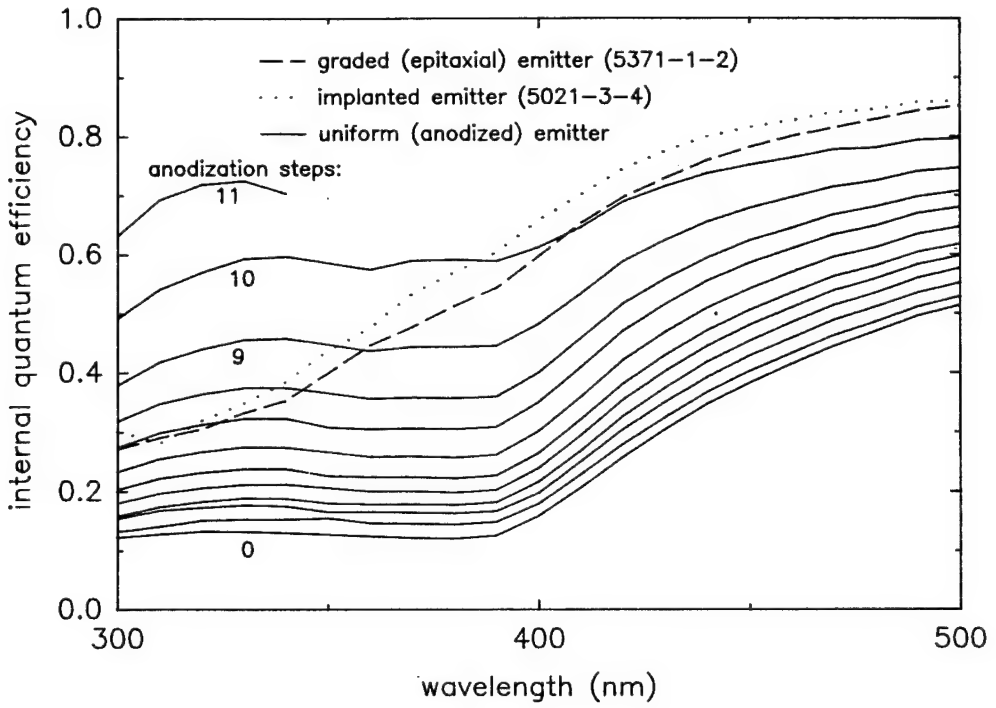


Figure 4-1 *Effect of anodization of the emitter. As the thickness of the emitter decreases, the collection efficiency in the blue end of the spectrum increases.*

Table 4-1 *Emitter Thickness Experiments. (Lots 5381, 5385)*

MOCVD run #	Emitter Growth time (s)	J_{sc} Before AR (mA/cm^2)	Eff. Before AR (%)	After AR (%)	Internal Q.E. @ 400 nm	Sheet Resistance (ohms)
1111 1116	100/100 70/70	23.65 24.62	12.68 13.01	19.14 n.a.	0.433 0.560	329 475
1124	100/100	24.17 ±0.12	12.91 0.10	17.39 0.17	0.530	n.a.
1127	130/70	25.07 ±0.10	13.42 0.05	18.05 0.31	0.624	n.a.

4.2.2 Emitter Doping

The requirement that the emitter be as thin as possible obviously requires, in turn, a high doping density. If the sheet resistivity of the emitter (which is inversely proportional to the thickness and the doping density), is too high, increased series resistance will result, lowering the fill factor of the cells. Sheet resistances up to 500 ohms can be accommodated in a 2 x 2 cell without too much difficulty, but values greater than 1000 ohms would require a different grid design, and would result in some additional losses.

To reach a sheet resistance of 500 ohms with a 20 nm thick emitter requires a doping density of approximately 6 x 10^{18} cm^{-3}. In the graded structure, in which the thickness of the most heavily doped layer is less, doping densities of 10^{19} cm^{-3} or greater are needed.

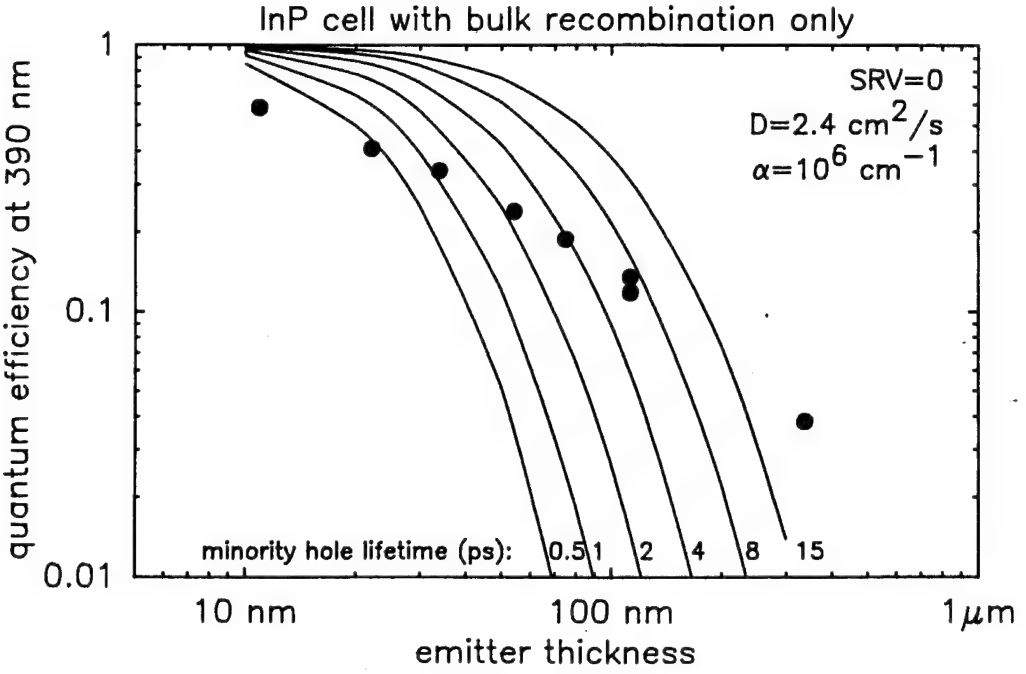
The measurements reported in Section 3.2.1 show that these requirements have been reached; layers up to 3 x 10^{19} cm^{-3} have been measured. Most of the solar cell runs used similar growth conditions to those of run #905, and had sheet carrier concentrations of 1.5 to 3 x 10^{13} cm^{-2}. Sheet resistances ranged from 300 to 500 ohms. While the difficulty of measuring thickness and actual dopant concentration prevented us from correlating these data from all of the solar cell runs, one experiment was carried out to observe the effect of a further increase in the dopant flow. This experiment showed no significant improvement; although the sheet resistances were slightly lower and the short-circuit currents the same, the effect on efficiency was negligible. Those results are presented in Table 4-2. We concluded that the lower dopant concentration (corresponding to 15 sccm) is sufficient.

Table 4-2 *Effect of Emitter Doping (Lot #5381).*

MOCVD run #	Emitter Dopant Flow (sccm)	J_{sc} Before AR (mA/cm^2)	Eff. Before AR (%)	After AR (%)	Internal Q.E. @ 400 nm	Sheet Resistance (ohms)
1111	15	23.65	12.68	19.14	0.433	329
1115	30	23.73 $\pm$0.05	12.68 $\pm$0.16	18.96 $\pm$0.24	0.457 $\pm$0.011	249 $\pm$43

The advantages of the graded emitter structure are also described in Section 3.2.1. These results provide support for the hypotheses which were advanced in the previous work. Using the data from the anodization experiment (Figure 4-2), values of surface recombination velocity and lifetime in the emitter were adjusted until the computed data matched the measurements. These results indicated that essentially all the recombination in the emitter took place at the front surface.

a)



b)

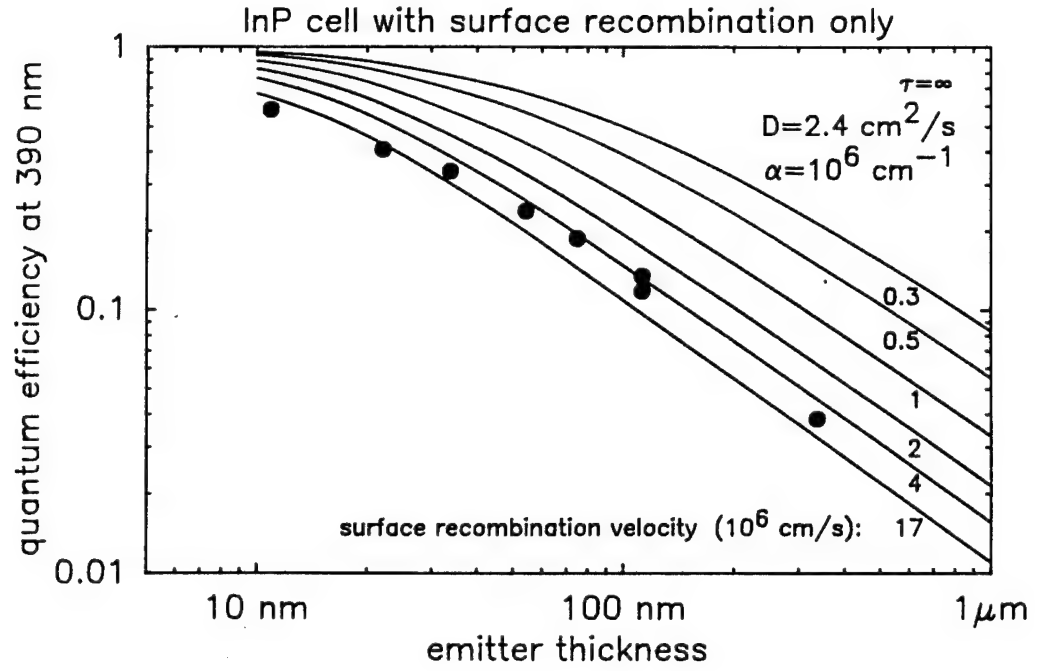


Figure 4-2 *Modeling of spectral response. The model with bulk recombination only; a) shows that any value of lifetime which fits the results from the shallow junctions will predict quantum efficiencies much too low for the deeper junctions. On the other hand, assuming that all the recombination takes place at the surface; b) yields predictions consistent with the data.*

Using this result in turn, the performance of graded emitter layers was projected by modeling, using Paul Basore's PC-1D code. Table 4-3, taken from the NASA final report, gives these results. Due to the remaining unknown factors, exact agreement with experiment can not be expected, but the calculated effects of the graded layer are qualitatively similar to those observed (Figure 4-3).

Table 4-3 *Theoretical Performance of Drift-field Cells (calculated with PC-1D).*

Structure	Layer	Thickness (microns)	Doping cm^{-3}	V_{oc} (mV)	J_{sc} (mA/cm^2)
1. Control	emitter base BSF	0.0320 3.0 0.5	10^{18} $2x10^{18}$ $5x10^{18}$	865.6	36.08
2. Graded emitter	emitter base BSF	0.0900 3.0 0.5	10^{18} - 10^{15} $2x10^{16}$ $5x10^{18}$	862.4	39.70
3. Graded emitter	emitter base BSF	0.0900 3.0 0.5	10^{19} - 10^{16} $2x10^{16}$ $5x10^{18}$	873.1	38.16
4. Graded base	emitter base BSF	0.0320 1.5 2.0	10^{18} 10^{15} - $5x10^{18}$ $5x10^{18}$	854.9	35.42
5. Graded base	emitter base BSF	0.0320 1.6 2.0	10^{18} 10^{16} - $5x10^{18}$ $5x10^{18}$	885.2	35.83
6. Graded both	emitter base BSF	0.0900 1.5 2.0	10^{18} - 10^{15} 10^{15} - $5x10^{18}$ $5x10^{18}$	850.5	38.64

4.2.3 Base Thickness

Throughout the early part of this work, a base thickness of 3 microns was used. This decision was based on the published absorption coefficients of InP and on the results of other investigators.[18,24] During this project, though, an experiment was done to assess whether that thickness is actually optimal. Cells were made using base thicknesses of 1.5 and 4 microns. Another structure was grown with the normal 3 μm base thickness, but with the thickness of the buffer layer (the layer underneath the base) increased from 0.5 microns to 2 microns. It was expected that the thinner base would show a lower red response, and the thicker base might show a slightly higher one. Results of these experiments are given in Table 4-4. It appears that 3 microns is necessary and sufficient for the base, and 0.5 microns is sufficient for the buffer layer.

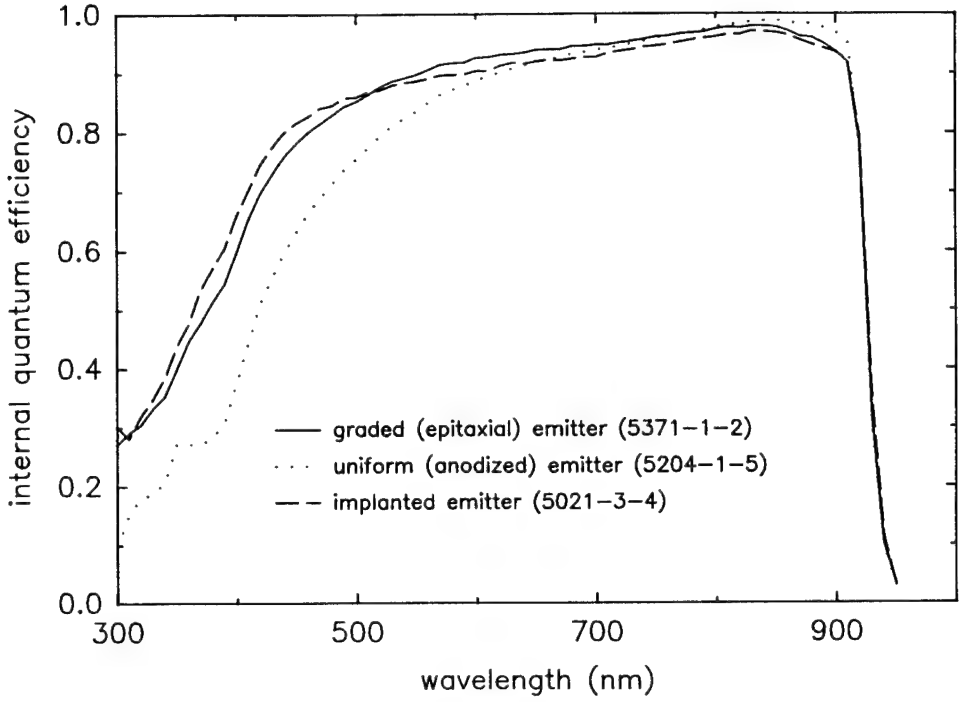


Figure 4-3 *Internal quantum efficiency of the epitaxial front-surface-field cell compared to previous epitaxial and implanted cells.*

Table 4-4 *Results of Base Thickness Experiments (Lots 5386, 5392).*

MOCVD run #	Base Thickness (μm)	Buffer Thickness (μm)	V_{oc} (mV)	J_{sc} mA//cm^2)	Eff. (%)	Internal Q.E. @ 850 nm
1126	3	0.5	865 ± 3	24.48 0.11	12.97 0.19	0.994
1128	4	0.5	869 ± 1	23.73 0.06	12.56 0.08	
1123	3	0.5	871 ± 2	24.10 0.23	12.81 0.25	0.983
1129	1.5	2	873 ± 1	23.34 0.12	12.47 0.11	0.915
1130	3	2	875 ± 2	23.79 0.16	12.74 0.37	0.963

4.2.4 Base Doping

The final cell parameter investigated in this project was the base dopant concentration. The base doping is of interest not only for obtaining the highest possible beginning-of-life efficiency, but also because published results have indicated that it has a strong influence on radiation resistance.[11]

The early work generally used a target of 3×10^{16} cm^{-3} for the dopant concentration, following published reports. However, occasional difficulties in controlling this parameter resulted in a considerable range, from about 3×10^{15} to 10^{17}, and the effect on the efficiency seemed to be small. Three experiments were done specifically to evaluate this effect; results are shown in Table 4-5. In addition, since the doping density of each completed cell was measured, we were able to combine the data into Figure 4-4, in which scatter plots of the open-circuit voltage and short-circuit current are shown as a function of doping density.

Table 4-5 *Base Doping Experiments (Lots 5363,5396, and 5415-17-18).*

MOCVD run #	Base Doping 10^{16} cm^{-3}	Before AR Coating			Internal Q.E. @ 850 nm	Reverse Saturation Current 10^{-16} Å/cm^2
		V_{oc} (mV)	J_{sc} (mA/cm^2)	Eff. (%)		
(Lot 5363)						
1058	2.5	871	23.57	12.43	0.985	0.46
1059	5.1	868	23.66	12.40	0.968	0.47
1060	5.5	874	24.16	12.88	0.969	0.43
1063	12	875	23.40	12.40	0.942	0.43
(Lot 5396)						
1134	4.7	875	24.10	12.78	0.985	0.38
(8 cells)	±0.2	1	0.26	0.10		
1131	8.0	872	23.85	12.68	0.971	0.40
(8 cells)	±0.5	2	0.16	0.26		
(Lot 5415)						
1168	6.6	876	24.82	13.12	0.982	0.37
(8 cells)	±0.8	1	0.08	0.25		
1167	18.5	882	24.54	13.01	0.954	0.29
(8 cells)	±2.8	1	0.10	0.17		
(Lot 5417)						
1058	1.8	870	24.10	12.79	0.978	0.48
(4 cells)	±0.7	1	0.10	0.10		
1059	5.2	866	12.32	12.32	0.960	0.56
1060	6.5	872	12.72	12.72	0.970	0.44
1063	14.1	872	12.37	12.37	0.929	0.43
(Lot 5418)						
1168-69	6.5	877	24.80	13.36		
(4 cells)	±0.8	2	0.11	0.05		
1171	17.1	882	24.43	13.28		
(4 cells)	±1.8	2	0.17	0.09		

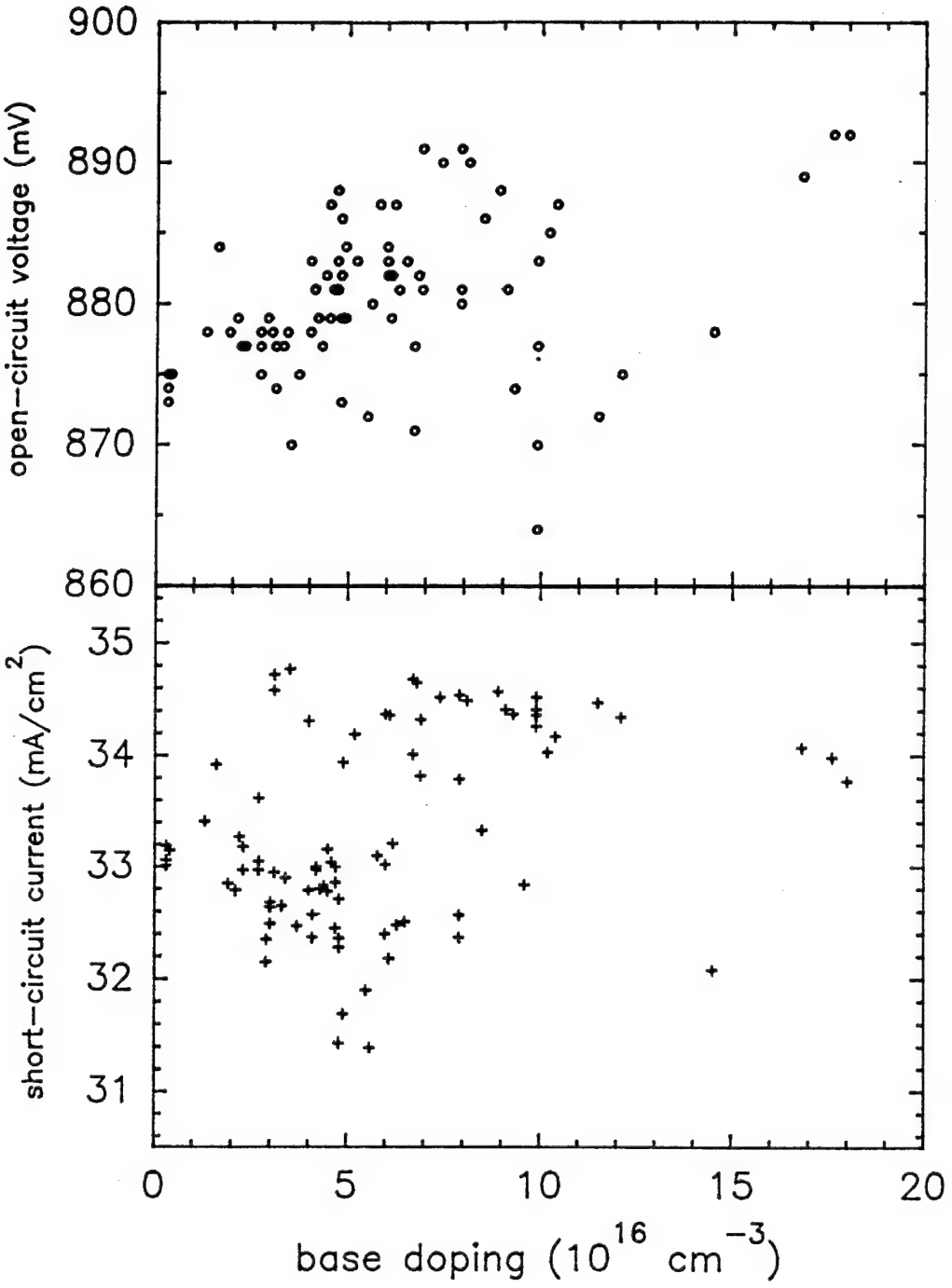


Figure 4-4 *Effect of base doping density. The highest voltages are seen in heavily doped cells; this improvement comes at the cost of a slight decline in voltage. It is also clear that there are other factors influencing the cell performance.*

Figure 4-4 shows considerable scatter in the data, since the V_{oc} and J_{sc} are influenced by factors other than the doping density. However, looking at the maximum values, we see the same trend which is evident in the data of Table 4-5: increasing doping density results in a slight increase in the V_{oc} and decrease in the J_{sc}, but these two effects tend to cancel one another, so the overall efficiency shows little if any dependence on base doping within the range investigated.

These results are consistent with the general theory of solar cells. Higher doping densities lead to lower saturation currents and thus to higher voltages. However, higher doping is usually associated with shorter carrier lifetime, which leads to lower current, particularly in the red end of the spectrum.

Cells with higher base doping are expected to have greater radiation resistance for two reasons: First, a carrier lifetime which is short to begin with will degrade less, but the high doping will still provide a lower saturation current. Second, carrier removal effects will become significant only when the number of removed carriers, which is generally a linear function of the radiation dose, is comparable to the original number of carriers.

4.3 PRODUCTION OF DELIVERABLE CELLS

In addition to advancing the understanding of the scientific issues involved in the design of InP solar cells, this project has also provided very valuable experience in the production of the devices. Figure 4-5 shows an efficiency histogram for a sample of 269 cells, which includes all of the deliverables and some additional cells produced in the course of this work. Figure 4-6 shows the I-V curve, measured at the NASA Lewis Research Center, of a selected cell.

4.3.1 MOCVD Growth Yield

In considering the yield in producing solar cells, we divide the process into three major areas: MOCVD growth, cell processing (which includes all steps after MOCVD growth up to the final coating and testing), and finishing, which includes sawing the cells to size, attachment of contact ribbons, coverglass application, and string and module assembly.

The yield in the MOCVD growth process is difficult to measure. Since many of the runs carried out were experiments, there were no expected results with which they could be compared. From time to time among the 80 solar cells runs performed, problems arose in the MOCVD process, resulting in obviously poor surfaces or inconsistent etching of the cap layers, but the number of such occasions is not great enough to give meaningful statistics.

Considering only the last 16 runs, which were done after the final process was established, no problems of this type arose. However, five of these runs appear to have resulted in lower cell efficiencies than expected (due to lower open-circuit voltage and fill factor). The evidence indicates that this resulted from a problem in MOCVD because wafers from different MOCVD runs were processed together, and the wafers from one run were normal, while the wafers from another showed low efficiencies (using the same batch of substrates). Also, the low efficiencies were found to be correlated with a low photoluminescence intensity. However, this problem had not been observed previously, so these sixteen runs do not appear to be representative of the process in general.

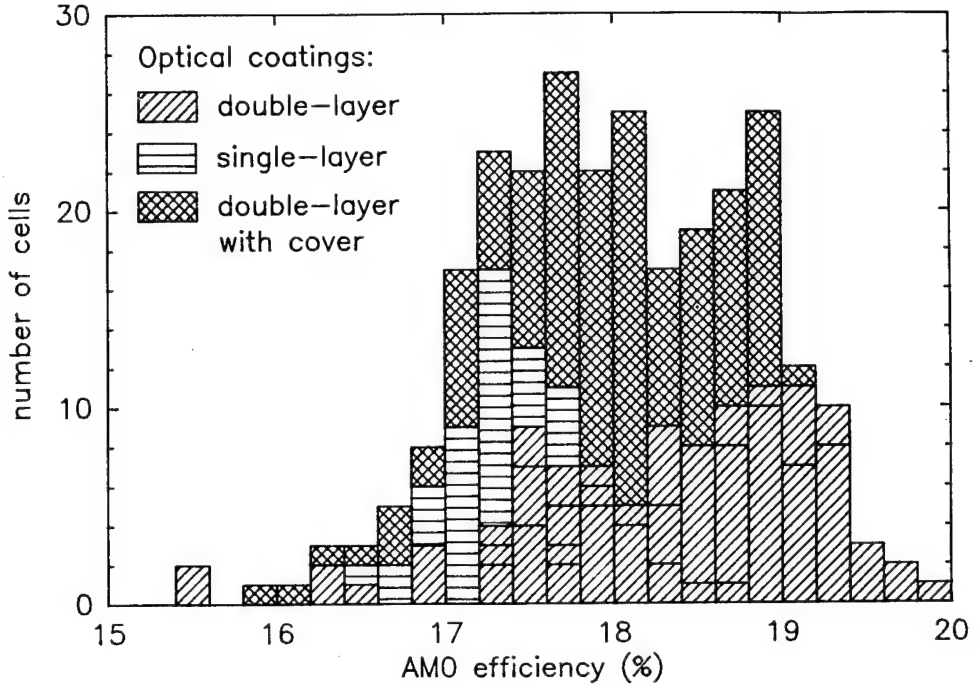


Figure 4-5 *Efficiencies of deliverable cells made in this project.*

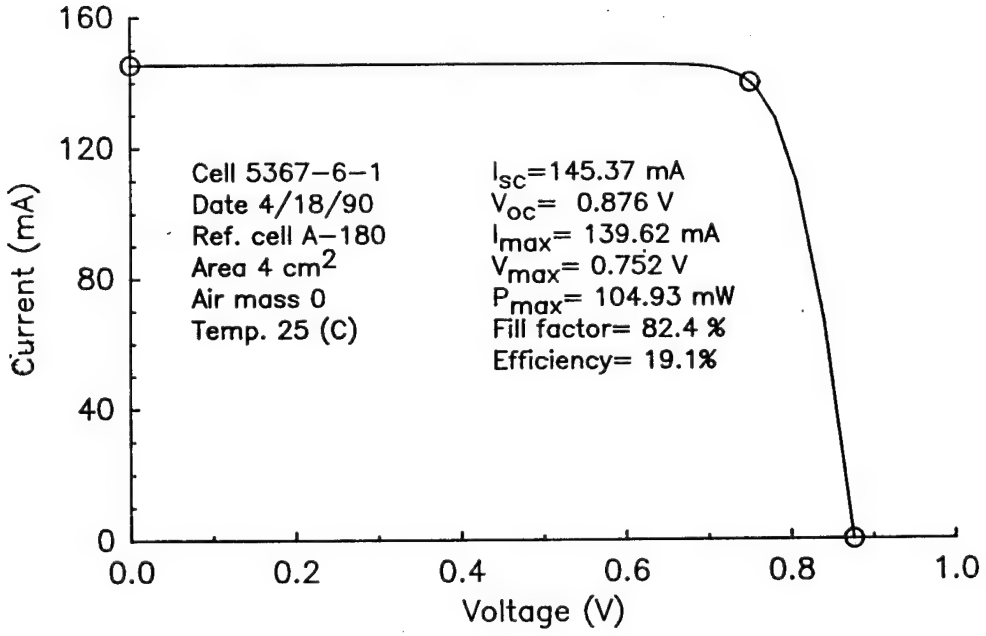


Figure 4-6 *I-V curve of the high-efficiency InP cell (measured by NASA Lewis Research Center).*

Identifying and solving this problem is clearly among the first tasks to be addressed in the next phase of development of the technology. Once this is solved, we can probably expect MOCVD yields of 90% or more.

4.3.2 Processing Yield

Great progress was made during this project in the yield of the cell processing area. In the beginning of this project, overall yields of 50% or less were obtained; many wafers were lost due to breakage. No specific problem area could be identified; in many cases, a cracked wafer would not be discovered until it was too late to determine exactly how it had been cracked.

Some of the changes made in the process seem to have contributed to solving this problem; eliminating the oxide coating step in the beginning undoubtedly did away with a large amount of stress on the wafers. Combined with more experience on the part of the technicians in handling the fragile wafers, these changes brought the yield for this area up to 88%, based on the last 103 wafers processed (Figure 4-7).

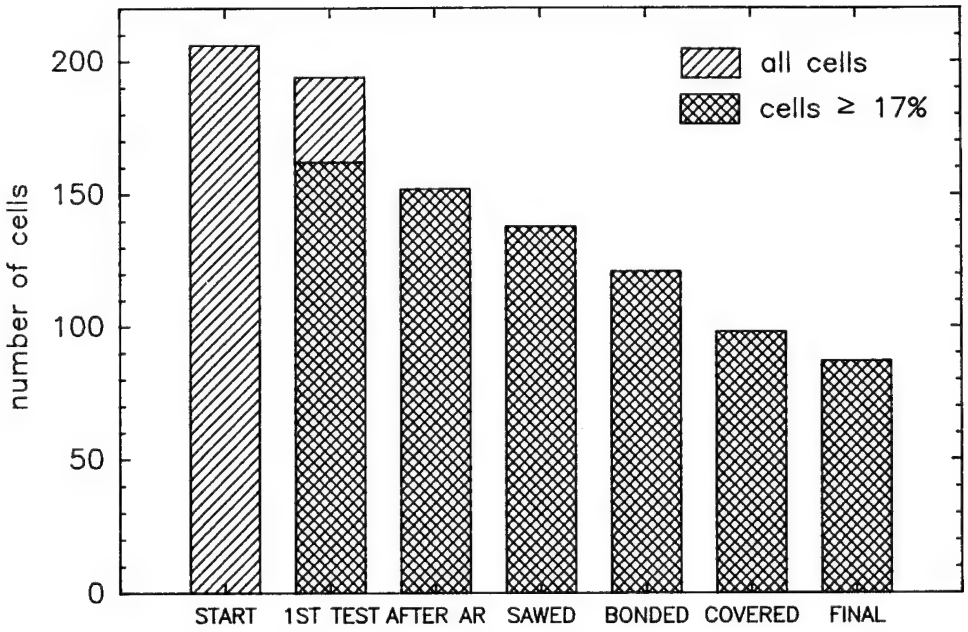


Figure 4-7 *Yield of solar cell fabrication by step. Some development is still required in sawing and related areas.*

4.3.3 Finishing Yield

Serious problems remain, however, in the finishing area. As shown in Figure 4-7, the overall yield from sawing to final inspection is only 57%. Since we began working on most of these processes only toward the end of the project, we might expect a somewhat lower yield here than in the previous steps, but observations indicate that there are still problems to be overcome.

As before, many cells were found to be cracked at the final inspection, at which point it could not be determined at what point they had first been damaged. Some evidence, however, points to the sawing step as the source of a large part of the damage; cracks have been seen to be associated with edge chips made by the saw blade. Further work on the sawing process is clearly indicated; further adjustment of the blade speed, blade type, and other parameters may lead to an improvement.

4.4 PANEL RESULTS

Two panels were made according to the procedures described in Section 3.3.3. Due to some mishaps which resulted in the broken cells, a total of four cells (in four different strings), had to be replaced after the assembly was completed. This was done by cutting the ribbons on either side of the broken cell, removing it from the adhesive, placing the replacement cell in its position with fresh adhesive, and soldering the ribbons to reconstitute the string. The replacement cell was first prepared with ribbons of the appropriate length.

After these panels were completed, each string was tested. Table 4-6 gives the test results, and compares them with the results calculated from the previously measured characteristics of the individual cells. The data were calculated for the temperatures at which the measurement was made, using temperature coefficients of -2.1 mV/K for the V_{oc} and 0.02 mA/cm^{2}K for the J_{sc}.

The results show that the lower voltages measured on the completed strings are attributable to the higher test temperature. However, the fill factors for the strings are also considerably lower than for the individual cells, and calculations indicate that the difference can not be accounted for by the temperature or by mismatch of the cell I-V characteristics. These low fill factors indicate a series resistance problem which presumably has to do with the interconnections.

The four strings which have been damaged and repaired do not seem to show a significant difference in this regard from the others. Thus it appears that the repairs are not the source of the problem. Analysis of the current flow on the back surface of the cell indicates that the resistance associated with the current flow into the soldered contacts (which are fastened to the cell at only two points) could explain the discrepancy. We do not expect this additional series resistance to interfere with the primary purpose of these panels: the measurement of performance and radiation sensitivity under actual space conditions.

Table 4-6 *InP Panel Results.*

String #	Temp. (°C)	Base Doping 10^{16} cm^{-3}	V_{oc} (mV)	I_{sc} (mA/cm^2)	Fill Factor	Eff. (%)	Substrate Material
*1(calc.)	25	1.5 - 6	4423	136.3	0.835	18.3	graphite
(calc.)	54		4171	138.2	0.820	17.2	
(meas.)	54		4129	140.1	0.778	16.4	
*2(calc.)	25	3 - 7	4415	136.1	0.840	18.4	graphite
(calc.)	52		4195	137.8	0.824	17.4	
(meas.)	52		4176	138.2	0.789	16.6	
*3(calc.)	25	3 - 3.5	4395	137.9	0.820	18.1	Al
(calc.)	30		4343	138.3	0.819	17.9	
(meas.)	30		4376	135.6	0.794	17.2	
4 (calc.)	25	5.5 - 7	4420	137.4	0.837	18.5	Al
(calc.)	33		4336	138.0	0.835	18.2	
(meas.)	33		4362	135.3	0.786	16.9	
5 (calc.)	25	5 - 6.5	4430	132.0	0.841	17.9	Al
(calc.)	32		4357	132.6	0.839	17.7	
(meas.)	32		4377	133.2	0.804	17.1	
6 (calc.)	25	14 - 20	4456	135.5	0.840	18.5	Al
(calc.)	35		4351	136.3	0.838	18.1	
(meas.)	35		4357	134.0	0.820	17.4	
7 (calc.)	25	0.3 - 6.5	4418	138.1	0.835	18.6	graphite
(calc.)	51		4208	139.7	0.819	17.5	
(meas.)	51		4191	137.2	0.801	16.8	
*8(calc.)	25	3 - 6.5	4402	135.6	0.830	18.1	graphite
(calc.)	70		3972	138.9	0.812	16.3	
(meas.)	70		4126	135.7	0.784	16.0	

* These strings required replacement of broken cells. All measurements are after replacement.

4.5 Environmental Testing

Two cells (5384-1-1 and 5385-2-1), with tabs and cover glasses, were subjected to ten temperature cycles from -60 to +100°C, to verify that the differential thermal expansion of the cell and the fused silica cover glass would not cause delamination or other problems. The cells were tested under the simulator and examined under the microscope before and after the thermal cycling treatment. A few small bubbles were seen before the treatment, and no change in either efficiency or appearance was observed.

Thermal cycling was also carried out with the two completed panels. Twenty-five cycles were carried out from -60 to +100°C, over a period of two days. Inspection afterward showed no damage to the cells or other panel components.

The panels were tested under the solar simulator before and after thermal cycling; results are shown in Table 4-7. Because the panels could not be mounted on a test block as are the individual cells, no temperature control was available for these tests, and so there was considerable variation of open-circuit voltage and short-circuit current. However, the small variation in fill factor between the two sets of measurements indicates that there was no significant damage to the panels from the thermal cycling test.

Table 4-7 *InP Panel Thermal Cycling.*

String #	Base Doping 10^{16} cm^{-3}	V_{oc} (mV)	I_{sc} (mA/cm^2)	Fill Factor	Eff. (%)	Substrate Material
1 (before)	1.5 - 6	4295	138.6	0.778	16.9	graphite
(after)		4129	140.1	0.778	16.4	
2 (before)	3 - 7	4334	136.7	0.784	16.9	graphite
(after)		4176	138.2	0.789	16.6	
3 (before)	3 - 3.5	4271	139.5	0.794	17.2	Al
(after)		4376	135.6	0.794	17.2	
4 (before)	5.5 - 7	4383	136.4	0.781	17.0	Al
(after)		4362	135.3	0.786	16.9	
5 (before)	5 - 6.5	4338	129.2	0.815	16.6	Al
(after)		4377	133.2	0.804	17.1	
6 (before)	14 - 20	4344	134.3	0.792	16.8	Al
(after)		4357	134.0	0.820	17.4	
7 (before)	0.3 - 6.5	4308	137.2	0.788	17.0	graphite
after		4191	137.2	0.801	16.8	
8 (before)	3 - 6.5	4212	136.1	0.766	16.0	graphite
(after)		4126	135.7	0.784	16.0	

4.6 RADIATION TESTING

In the first set of radiation tests, 21 cells (8 4 cm^2 and 13 0.25 cm^2) were subjected to 1 MeV electrons. Doses of 10^{14}, 4 x 10^{14}, 10^{15}, and 10^{16} electrons/cm^2 were used. The dose rate was approximately 2 x 10^{12} electrons/cm^2/sec.

The cells were measured before and after each dose. Control cells were measured at the same time and used to correct for any drift in the simulator calibration. Spectral response and dark I-V curves were taken of selected cells.

These cells were all taken from Lot # 5374 (MOCVD run 1108 and 1109), and all had base doping concentrations in the neighborhood of 6 x 10^{16} cm^{-3}. Efficiencies before irradiation varied from 17.5% to 19.6%.

All of the irradiated cells showed measurable degradation. The relative loss was roughly evenly divided between the open-circuit voltage and the short-circuit current; the fill factor changed somewhat less. Table 4-8 shows the results from a typical cell; the variation in the degradation from cell to cell was small.

Table 4-8 *Results of First InP Cell Irradiation (Cell # 5374-2-2, 4 cm^2).*

Dose (cm^2)	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Efficiency (% AMO)	Degradation (%)
0	886	34.82	0.840	18.9	0.0
1E+14	862	34.27	0.842	18.1	4.2
4E+14	835	33.09	0.819	16.5	12.7
1E+15	813	32.44	0.813	15.6	17.5
1E+16	750	29.25	0.751	12.0	36.5

Detailed analysis of the irradiated cells showed, as expected, a decrease in the collection efficiency for long-wavelength light resulting from the reduction in diffusion length, and also an increase in the reverse saturation current resulting from the decreased lifetime, particularly in the space-charge region (Table 4-9).

Table 4-9 *Results of First InP Cell Irradiation (Cell # 5374-2-2, 4 cm^2).*

Dose (cm^2)	Q.E. @ 850 nm	J_0 (n=1.0) (10^{-16} Å/cm^2)
0	0.984	0.38
1E+14	0.954	0.82
4E+14	0.906	3.0
1E+14	0.831	6.7
1E+16	0.640	32.3

To elucidate the effect of the base doping density on the radiation resistance of the cells, a second group of 14 cells was irradiated. These cells had base doping varying from 3 x 10^{15} to 2 x 10^{17} cm^{-3}. As can be seen from the results in Table 4-10, the doping density had an interesting effect on the degradation of the cells. The lightly-doped cells show almost no loss of short-circuit current (3%), whereas the heavily-doped cells show a considerable loss (22%). On the other hand, the lightly doped cells show much more loss of voltage than the heavily-doped cells.

Table 4-10 *Effect of Base Doping Density.*

Cell #	Doping (cm^{-3})	Dose (cm^{-2})	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Efficiency (% AM0)
5412-2-4	$3x10^{15}$	0	874	34.00	0.838	18.1
		10^{14}	850	33.93	0.797	16.8
		$4x10^{14}$	805	33.90	0.782	15.6
		10^{15}	764	33.87	0.775	14.6
		10^{16}	666	33.10	0.721	11.6
5416-1-5	$6x10^{16}$	0	888	34.42	0.839	18.7
		10^{14}	853	33.84	0.824	17.3
		$4x10^{14}$	822	32.79	0.817	16.0
		10^{15}	803	31.52	0.801	14.8
		10^{16}	745	28.36	0.749	11.5
5415-2-5	$2x10^{17}$	0	894	33.90	0.819	18.1
		10^{14}	870	33.15	0.817	17.2
		$4x10^{14}$	845	31.90	0.799	15.7
		10^{15}	825	30.45	0.659	12.1
		10^{16}	772	26.57	0.738	11.0

The explanation of this phenomenon has to do with the width of the space-charge region, which is much greater in the lightly-doped cells. Since carriers generated in the space- charge region itself are subject to an electric field, they are collected more quickly than carriers generated in the base. Thus, the short carrier lifetime in the radiation-damage material does not strongly degrade the collection efficiency for these carriers.

In the case of the heavily-doped cells, the space charge region width is 90 nm, meaning that only 66% of the light is absorbed in that region and the emitter together. (The emitter, which is 30 nm thick, absorbs 34%.) In the lightly-doped ($3x10^{15}$ cm^{-3}) cells, the corresponding values are 750 nm and 96%. In fact, because of compensating donors introduced by the radiation damage, the net doping density of the lightly-doped cells after irradiation is even lower than the 3 x 10^{15} cm^{-3} measured beforehand; capacitance measurements indicate a space-charge region width of 1.5 microns after irradiation: enough to absorb 98% of the light.

Because of the width of the space-charge region in this case, it becomes the dominant site for recombination at open-circuit as well as absorption. The diode shows non-ideal behavior (n=2) and the reverse saturation current is proportional to the space-charge region width. This measured saturation current is given as J_{02} in Table 4-11; it explains the difference in voltage between the lightly-doped and heavily-doped irradiated cells.

Table 4-11 *Effect of Base Doping Density.*

Cell #	Doping (cm^{-3})	Dose (cm^{-2})	Q.E. @ 850 nm	J_{02} (10^{-10} Å/cm^2)
5412-2-4	$3x10^{15}$	0 10^{16}	0.9877 0.9685	 120
5416-1-5	$6x10^{16}$	0 10^{16}	0.9833 0.6411	 4.1
5415-2-5	$2x10^{17}$	0 10^{16}	0.9589 0.5651	 5.3

This analysis indicates that the cell thickness can be an important parameter for optimum design of the cell under conditions of radiation damage. 500 nm of InP is enough to absorb 92% of the incoming light; lightly-doped cells with that thickness would be expected to show approximately 50 mV higher voltage after irradiation than those reported here (because of the reduced space-charge-region recombination), at a small cost in current.

It is interesting to compare these lightly-doped cells, which, after irradiation, are essentially n+-i-p cells, with the results of workers at NTT, who investigated a p+-i-n structure.[25] The NTT workers found that the radiation resistance of the p+-i-n structure was inferior to that of the n+-p-p+ cells which are more similar to the heavily-doped cells used here; the voltage degraded more quickly with irradiation. While that is also the case with our n+-i-p cells, the resistance of the current to degradation compensates for that disadvantage. Although the NTT workers did not publish the details of their structure or measurements, it seems likely that their emitter (p+ layer) is thicker than ours (n+ layer), and thus a larger fraction of the light is absorbed in the emitter and a smaller fraction in the space-charge region. This would explain the fact that they apparently observed considerable current degradation and we did not.

4.7 ANNEALING

Various annealing experiments were performed on selected irradiated cells. Room temperature, elevated temperature, forward bias current, and light illumination were investigated for their annealing properties.

Room-temperature annealing was observed in all of the cells; Table 4-12 shows typical results. Roughly one quarter of the damage in the more heavily-damaged cells was recovered at room temperature after about six weeks, and roughly one half of the damage in the less heavily-damaged cells (4×10^{14} cm^{-2}).

Table 4-12 *Room-temperature Annealing.*

	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Efficiency (% AM0)	Degradation (%)
	(Cell # 5374-2-2, 4 cm^2)				
Before irradiation	886	34.82	0.840	18.9	
After radiation (10^{16} electrons/cm^2)	750	29.25	0.751	12.0	36.5
After 384 hours	756	29.78	0.755	12.4	34.4
After 1128 hours	762	30.39	0.770	13.0	31.2
After 7776 hours	763	30.89	0.764	13.1	30.5
	(Cell # 5374-8-1, 4.00 cm^2)				
Before irradiation	889	34.83	0.842	19.0	
After irradiation ($4x10^{14}$ electrons/cm^2)	834	32.73	0.761	15.2	20.2[a]
After 384 hours	844	34.34	0.828	17.5	7.9
After 1128 hours	846	34.82	0.822	17.7	7.0
After 11 months	846	34.25	0.833	17.6	7.4

[a] The fill factor of this cell showed more degradation than the typical case; this may represent a measurement error.

Annealing at elevated temperature was somewhat more effective. At 60°C, the cells recovered about the same amount as at room temperature, but in only one week. At 137°C for 30 minutes, slightly more damage was recovered than at room temperature, although recovery was still not complete (Table 4-13). Annealing at 180°C showed no improvement over annealing at 140°C, but annealing at 300°C gave significantly more recovery.

Annealing with current and with light appeared to be slightly more effective than annealing at room temperature, but less effective than annealing at 137°C (Table 4-14).

Table 4-13 also shows the corresponding annealing results from the second group of radiation tests; these cells were annealed at 140°C and 300°C for 30 minutes. The data show that the heavily-doped and lightly-doped cells show roughly equal recovery in open-circuit voltage, but that the lightly-doped cell (which is effectively a p-i-n device at this point) shows essentially complete recovery of the short-circuit current, resulting in a significantly higher efficiency after the irradiation and anneal cycle.

Table 4-13 Annealing at Higher Temperatures.

	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (% AM0)	Degradation (%)
	(Cell # 5374-1-4, 0.25 cm^2)				
Before irradiation	888	34.42	0.841	18.7	0.0
After radiation (10^{16} electrons/cm^2)	740	28.04	0.746	11.3	39.6
After 24 hours @ 60°C	763	29.58	0.734	12.1	35.3
After 72 hours @ 60°C	764	29.77	0.784	13.0	30.5
After 168 hours @ 60°C	765	30.51	0.773	13.1	29.9
	(Cell # 5374-2-4, 0.25 cm^2)				
Before irradiation	889	35.89	0.846	19.7	0.0
After irradiation (10^{16} electrons/cm^2)	740	28.54	0.751	11.6	41.1
After 10 min. at 137°C	770	29.98	0.766	12.9	34.6
After 30 min. at 137°C	775	30.95	0.781	13.7	30.7
	(Cell # 5374-5-4, 0.25 cm^2)				
Before irradiation	881	34.93	0.823	18.5	0.0
After irradiation (10^{16} electrons/cm^2)	744	28.44	0.747	11.5	37.8
After 30 min. at 100°C	771	31.11	0.779	13.6	26.5
After 30 min. at 140°C	779	31.58	0.780	14.0	24.3
After 30 min. at 180°C	779	31.78	0.775	14.0	24.3
	(Cell # 5412-2-4, 0.25 cm^2, low base doping)				
before irradiation	874	34.00	0.838	18.1	0.0
after irradiation (10^{16} electrons/cm^2)	666	33.10	0.721	11.6	35.9
After 30 min. at 140°C	736	34.04	0.754[a]	13.8[a]	23.8
After 30 min. at 300°C	809	34.03	0.792	15.9	12.2
	(Cell # 5415-3-4, 0.25 cm^2, high base doping)				
before irradiation	891	33.17	0.849	18.3	0.0
after irradiation (10^{16} electrons/cm^2)	780	25.81	0.750	11.0	39.9
After 30 min. at 140°C	803	27.76	0.779[a]	12.7[a]	30.6
After 30 min. at 300°C	820	28.62	0.806[a]	15.5[a]	15.3

[a] Fill factors of these cells were calculated from dark I-V curves instead of measured directly.

Table 4-14 *Effect of Light and Current Anneals.*

	V_{oc} (mv)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (% AM0)	Degradation
	(Cell # 5374-2-5, 0.25 cm^2)				
Before irradiation	890	35.56	0.849	19.6	0.0
After irradiation (10^{16} electrons/cm^2)	733	28.28	0.759	11.5	41.3
After 384 hr @ RT	753	29.31	0.761	12.2	37.8
After current injection 5 min. @ 30 mA	761	29.43	0.758	12.4	36.7
	(Cell # 5374-3-4, 0.25 cm^2)				
Before irradiation	873	35.38	0.842	19.0	0.0
After irradiation (10^{16} electrons/cm^2)	747	27.54	0.755	11.3	40.5
After 384 hr RT	761	28.76	0.763	12.2	35.8
After light injection 20 min. 1-sun AM0	770	29.39	0.755	12.5	34.2

Figure 4-8 shows the efficiency loss of the first group of irradiated cells with radiation dose and their recovery with annealing. Figure 4-9 compares these data with corresponding measurements made by other research groups working with InP and GaAs solar cells. The efficiencies we measured after the higher doses of radiation are very close to those measured by others in InP, and the beginning-of-life efficiencies are higher. Comparing the InP data to GaAs, we see similar efficiencies after 10^{15} cm^{-2} electrons, but higher efficiencies after 10^{16}, despite slightly lower beginning-of-life values.

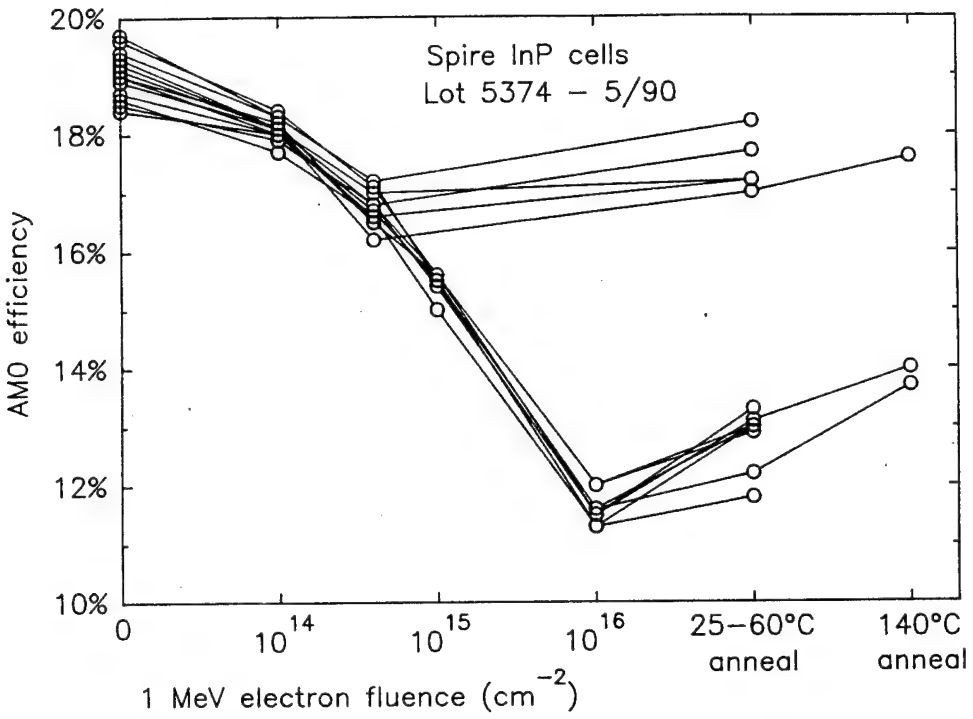


Figure 4-8 *AM0 efficiency of InP cells from this work after irradiation and annealing. Some cells received only $4x10^{14}$ cm^{-2} dose, and some 10^{16} cm^{-2}; effects are shown for all of these cells after 7 days at room temperature and after 30 minutes at 140°C.*

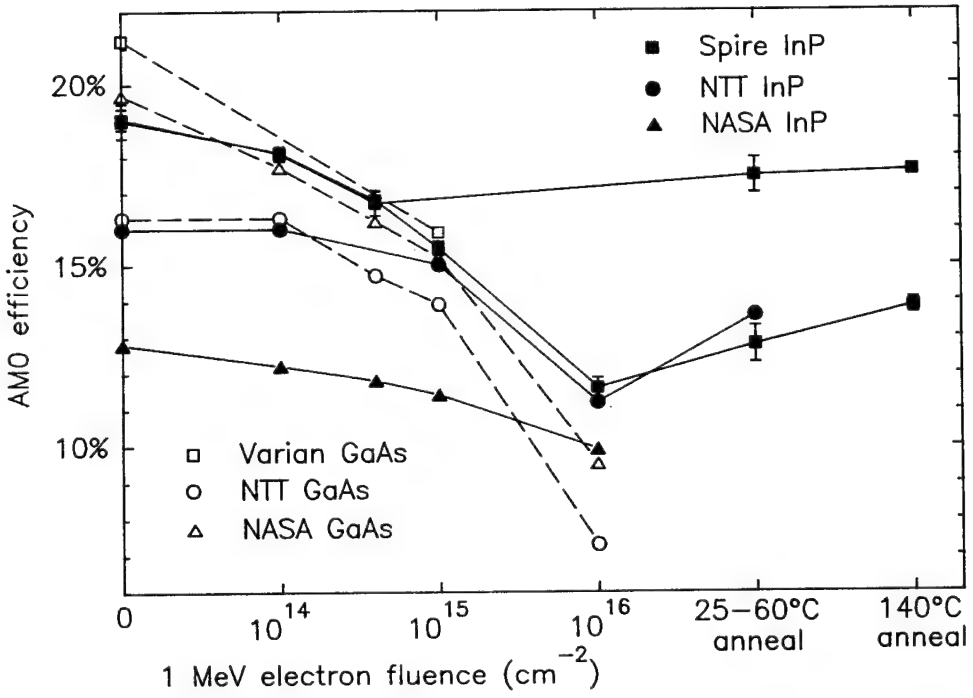


Figure 4-9 *Spire radiation testing data compared to those published by other researchers in InP and GaAs.*

SECTION 5
CONCLUSIONS

5.1 CELL STRUCTURE AND EFFICIENCY

This project has determined what is essentially the optimum structure for the shallow-homojunction InP solar cell given the current state-of-the-art in MOCVD growth techniques. Further changes in the thickness and doping of the base and emitter layers could be investigated, but the data we have suggest that further gains in efficiency from such incremental improvements would be small.

The highest conversion efficiency verified at NASA was 19.1%. (Figure 4-7) Although values as high as 19.8% have been measured at Spire, the difference in measurement and calibration conditions makes those values somewhat questionable. The highest efficiency measured on a cell with a coverglass was 19.1% (26.2 mW/cm^2). Our experience indicates that 20% may be possible in the laboratory, but should be considered an upper limit for the shallow-homojunction device. 18% in production is probably a reasonable goal at this point.

The radiation tests show a typical end-of-life efficiency of 11-12% after 10^{16} 1 MeV electrons/cm^2; this is considerably greater than reported for the best GaAs cells, which have higher efficiencies at the beginning.[26] The efficiency after 10^{15} electrons/cm^2 is 15-16%, about the same as GaAs. We can expect, then, that for applications with a radiation dose in this range, InP currently provides the highest end-of-life efficiency of any known material. This could make InP the first choice for some space missions already, and any further improvements in InP cells, if they are reflected in the end-of-life efficiency, could make it more attractive even for lower-dose missions.

5.2 PRODUCTION YIELD AND CAPACITY

The experience gained in this contract has been invaluable in preparation for production of InP solar cells. Inefficient process steps, such as anodization, have been eliminated so that all steps will be amenable to scale-up.

Losses due to breakage have been reduced to acceptable levels; at this point we can expect a yield of at least 75% up to the final coating and testing. Although the sawing, tabbing, and covering operations still have some problems, we expect that further experience will improve the yield there considerably.

The factors controlling the production capacity have also been identified. The MOCVD growth is done in batches of five wafers, and each run takes 3.5 hours, including loading, heating, cooling and unloading time; one additional hour is required for cleaning the reactor chamber. Thus, two runs per day should be possible by arranging shifts appropriately. Larger reactors, which are still in developmental stages, would of course increase the capacity, although using large reactors with phosphorus compounds is expected to raise additional problems in maintenance, cleaning, and effluent treatment.

Most of the post-growth processes are easily adaptable to higher volumes. Etching, annealing, and metal liftoff steps can easily be carried out in larger batches, limited only be the size of the vessels available. Photolithography is somewhat slower, but throughput of 10 wafers per hour can be achieved with a typical aligner. Sawing is also an individual process, and, as explained in Section 6.1.1, some further development work is required in that area, but we expect throughput of 10 wafers per hour also.

The rate-limiting steps are likely to be the evaporations. The process as currently established requires four evaporation steps: back contact, front contact, and two separate layers for the antireflection coating. This can probably be reduced to three, but it will still represent a considerable bottleneck. The front contact evaporation requires approximately one hour to deposit the thick (5 micron) layer of silver required. Although the other evaporation steps require much thinner layers, the time needed for evacuating the chamber can be two hours or more. The evaporators used for this research project have capacities of about 8 wafers per run. This was sufficient for research purposes, but it is clear that much larger equipment will be needed for production.

SECTION 6

DIRECTIONS FOR FURTHER DEVELOPMENT

6.1 FURTHER DEVELOPMENT OF CURRENT PROCESS

This project has made great progress in developing an efficient, reliable process for manufacture of InP solar cells. However, there are still a few minor problems which have arisen and will need to be solved.

6.1.1 Sawing

The most important of these is the high breakage rate observed in the finishing processes (sawing, bonding, and covering). We attribute much of this to the sawing step; it appears that the sawing introduces small cracks and chips which cause the cells to break later in the process. Figure 6-1 shows such a chip and an associated crack. Adjusting the parameters of the sawing process is one possibility for reducing this damage to acceptable levels; if this is not successful, other ideas such as the use of an etching step after sawing can be tried.

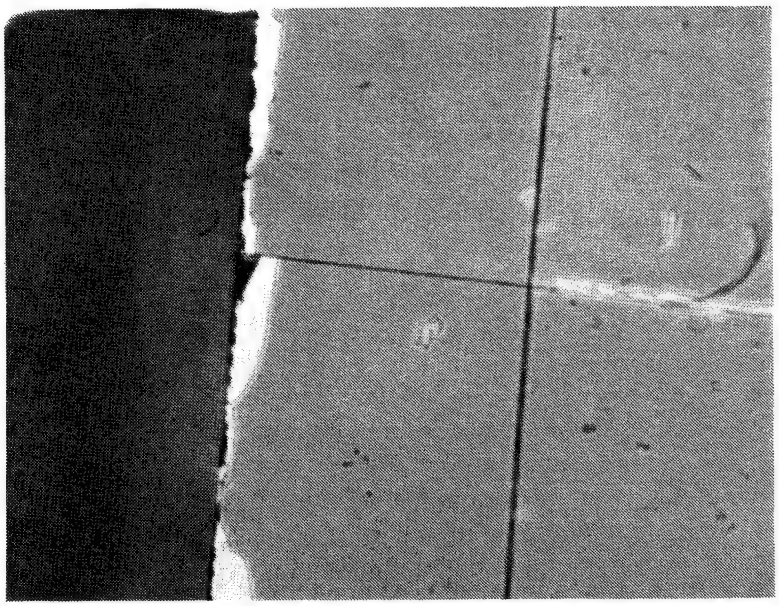


Figure 6-1 *Saw damage to InP solar cell. This photograph shows the edge of a cell which has been cut by the saw. The irregularities can act as sources for cracks.*

6.1.2 Front Contact Development

Further improvement of the front contact adhesion appears to be desirable, based on some problems which have arisen in handling of completed cells. Investigation of annealing steps after the front contact deposition, and of more effective diffusion barriers than the Au layer which was used here, may yield some progress. Before this can be addressed in a scientific manner, however, a qualitative method of measuring the adhesion, and possibly a corresponding standard, must be established.

6.1.3 Thinning

Reducing the thickness of the final cell is clearly desirable, since it will result in reduced cell weight with no effect on the efficiency. Two approaches could be used to solve this problem. Since, in the development of the back contact, it has proved possible to make the contact at a relatively low temperature (420°C), it may be possible to thin the wafer or cell after all the other processing is completed, and apply the back contact after thinning. This is the simpler process, but it must be verified that it is compatible with the front metallization.

If the front contact can not survive the temperature for back contact formation, then thinning must be done earlier in the process. In this case, the patterned thinning approach, which Spire has used in the past for 2 mil thick silicon cells, may be used. In this process, a mask on the back of the wafer is used to thin the cell area to the desired thickness, while keeping the edges of the wafer considerably thicker (Figure 6-2). The thick edges allow easier handling of the wafer, and, after processing is completed, they are removed by sawing.

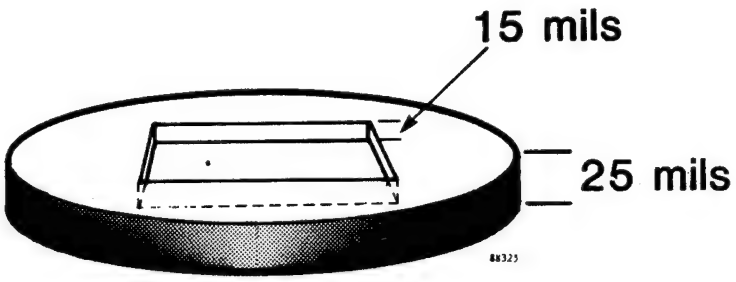


Figure 6-2 *Patterned thinning approach, which could be used to manufacture thin InP cells. The cell area is thinned from the back of the wafer, and the thick edges of the cell allow for handling without excessive breakage.*

6.2 RADIATION EFFECTS MEASUREMENT

The radiation and annealing tests done under this project have established the rate of degradation under laboratory conditions. However, it has become clear through this work and other results that radiation damage and annealing is very complex, i. e., that there are significant dependences on dose rate, temperature, and illumination conditions. Thus, in order to quantify accurately the radiation resistance of these InP solar cells, the actual use conditions must be duplicated as closely as possible.

The laboratory irradiation tests done in this project should be repeated with the irradiation performed under illumination equivalent to AM0 and at the temperature expected during operation in space. The degradation under these conditions should be compared with that measured at room temperature under the normal low illumination levels used here.

Although this experiment will give a considerably improved projection of the actual end-of-life efficiency, there is of course no substitute for actual space testing. In this case, testing should be done in relatively high-radiation orbits, so that data can be gathered in a short time and extrapolated to longer periods in lower-radiation orbits. Such tests are currently planned, using cells made in the course of this project, and the data from them will be essential for planners who are to decide between the types of solar cells available for future space missions.

6.3 INCREASE IN PRODUCTION CAPACITY

The development needed to scale up InP cell production to higher levels, as described in Section 5.2, will be mostly straightforward. All of the processing steps after MOCVD growth are common in the solar cell and semiconductor device industries, and equipment for carrying them out with a high throughput is commercially available.

Although increasing the capacity of MOCVD reactors is far from trivial, plans are in place to do so for solar cell applications. Figure 6-3 shows a series of proposed reactors which Spire has begun to design for production levels of GaAs solar cells.

Two areas, however, require new technology which must be developed. First, the MOCVD growth of InP has not been the subject of as much development work as that of GaAs, and it presents some problems which are different from those of GaAs.

Especially for large MOCVD chambers, which require high flow rates of phosphine, the effluent treatment presents a problem. Although phosphorus is not as toxic as arsenic, it is more corrosive and is extremely flammable. In the course of MOCVD growth, it deposits on the chamber walls and in other parts of the plumbing downstream from the chamber. We have found that careful design of the vacuum system is essential to prevent damage from the phosphorus deposits, and that deposits on the chamber walls can interfere with throughput. While we have these problems well in hand with the five-wafer reactor we are currently using, slightly different approaches may be needed for larger machines. In particular, a warm-wall system may be the most efficient, since it prevents or reduces condensation of phosphorus on the chamber walls. However, this results in greater amounts of phosphorus in the exhaust plumbing, and some further development will be needed to find the best way of handling that effluent.

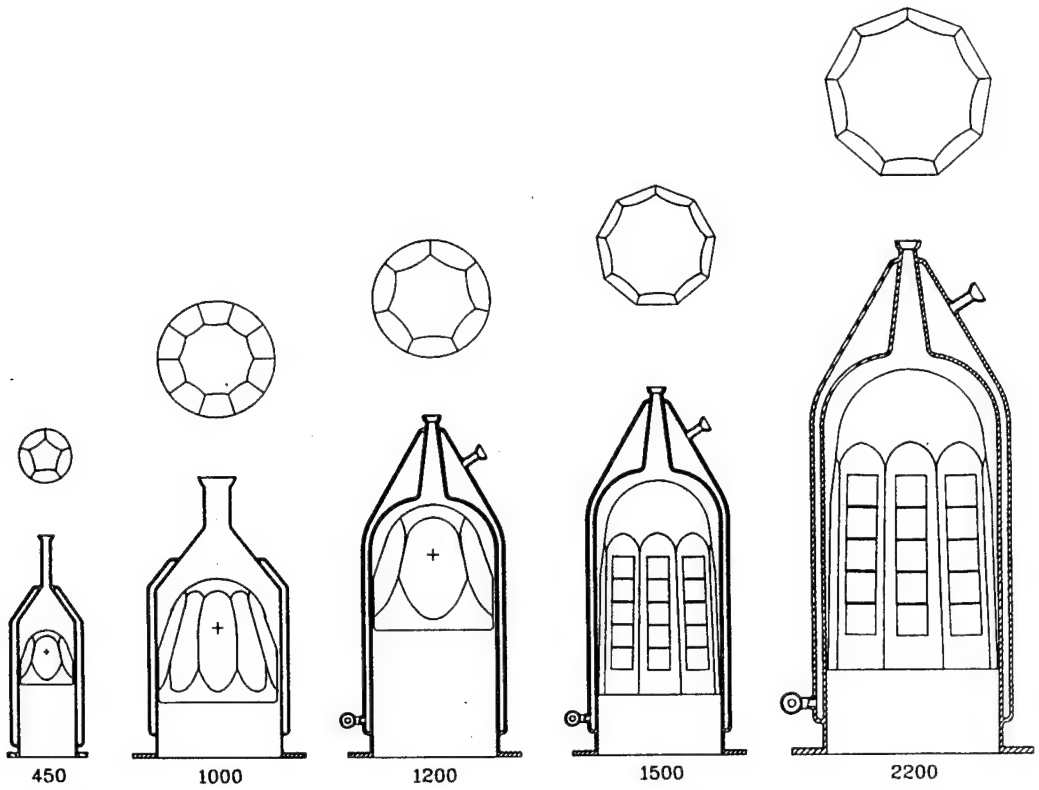


Figure 6-3 *Planned large-scale MOCVD reactors for solar cell production. The model 1500 is to have a capacity of 45 5 cm square substrates.*

The other concern for production levels of InP solar cells is the supply of substrates. Since this project did not include any development related to substrate manufacture, we do not have specific information concerning the equipment and labor requirements to produce substrates at the rate needed for solar cell production. Considering that InP is generally a smaller industry than GaAs, though, it is not clear how easily the increase in demand for cell production could be met, or what the cost would be. This is clearly something that must be carefully considered in any plans to start production of cells.

6.4 OTHER SUBSTRATES

Another approach which has the potential to solve the problems of substrate cost and availability is the heteroepitaxial growth of InP on another substrate, for which silicon is probably the most obvious choice. We are currently working on this idea under NASA funding.

Growth of InP on silicon has been carried out, but the large lattice mismatch results in a high density of defects in the InP film, which result in an efficiency penalty. As has been done with some success in the related area of GaAs-on-Si, various growth techniques can be used to reduce the defect density. Also, the use of a Bragg reflector with a thinner-than-normal InP cell structure can make the cell performance less sensitive to the defect density.

Figure 6-4 shows the calculated efficiency of an InP-on-Si cell, compared with recent experimental results. If the dislocation density can be reduced to 10^5 cm^{-2} or less, efficiencies essentially the same as those with InP substrates should be possible. Even at 10^6 cm^{-2}, the efficiency penalty may be small enough to make the structure cost-effective, particularly after irradiation. Bragg reflectors improve the situation further.

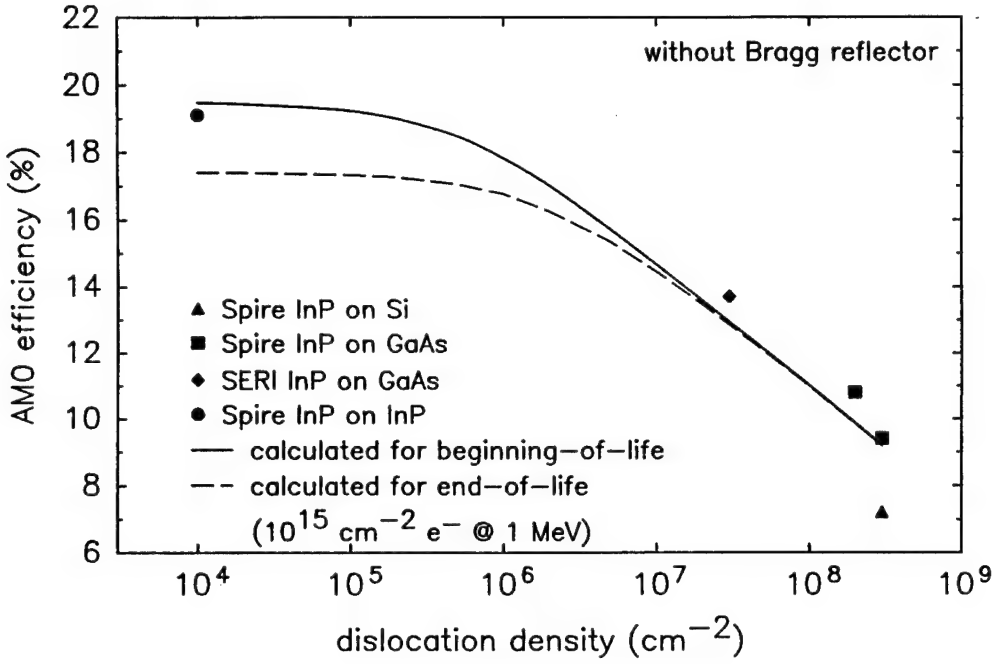


Figure 6-4 *Calculated efficiency of InP-on-Si solar cells. If the dislocation density can be reduced to about 10^5 cm^{-2} or less, the efficiencies essentially the same as those using InP substrates should be possible.*

6.5 WINDOW LAYERS

InP solar cell development is now approaching the limits of the shallow-homojunction structure. Substantial further improvement, to efficiencies of 21-22%, is possible, but will require some form of surface passivation.

The most promising approach to surface passivation, which has been successful with GaAs cells, is to use wide-bandgap window layers to reduce the recombination at the surfaces (Figure 2-6), according to the same principle which is used for heterostructure lasers. This layer reduces the surface recombination velocity and makes possible efficient collection of the current absorbed in the emitter, and also allows higher open- circuit voltages. Although there is some loss of current due to absorption of light in the window layer, our calculations indicate that, if the window thickness is kept to a minimum (50 nm), the effects of the reduced surface recombination more than compensate for this loss.

Table 6-1 shows projections of possible efficiencies under the assumption that the surface recombination velocity can be reduced to 10^5 cm/s with a window layer. Calculations show that only heterostructures can promise to meet the efficiency goal of 20% AM0 in practice.

Table 6-1 *Potential Efficiency for InP Cells with Passivation.*

Cell Parameter	Current Value	Future DH Cell	Theoretical Maximum	Limited By
Open circuit voltage (mV)	876	930	950?	band-gap narrowing
Short-circuit current (mA/cm^2)	36.3	37.9	42.7	Front surf. recombination absorption in window
Fill factor	0.824	0.855	0.878	Series resistance
Efficiency (%)	19.1	22.0	26.0	

Unfortunately, there is no convenient ternary compound analogous to AlGaAs which is lattice-matched to InP. Two candidates have been identified: $AlAs_{.56}Sb_{.44}$ and CdS. The former has the disadvantages that it is not a well-known material, so considerable development work would be needed to establish the parameters for growth, and it is expected to be very sensitive to air and moisture.

Cadmium sulfide (both epitaxial and polycrystalline) has been used for heterojunction solar cells in the past,[27-29] both in InP and other materials. It has a direct bandgap of 2.42 eV and about 0.8% lattice mismatch with InP. (The ternary $CdS_{.82}Se_{.18}$ is expected to give an exact lattice match with a bandgap of about 2.3 eV.) It can be deposited by evaporation, and, while CdS-on-InP epitaxy is not a routine process, much of the groundwork for this structure has been done. This leads us to conclude that it is the most promising approach for achieving InP efficiencies comparable to those already reached with GaAs.

SECTION 7

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